A Modelling and Nonlinear Equalization Technique for a 20 Gb/s 0.77 pJ/b VCSEL Transmitter in 32 nm SOI CMOS

Mayank Raj, *Student Member, IEEE*, Manuel Monge, *Student Member, IEEE*, and Azita Emami, *Member, IEEE*

***Abstract*—This paper describes an ultralow-power VCSEL transmitter in 32 nm SOI CMOS. To increase its power efficiency, the VCSEL is driven at a low bias current. Driving the VCSEL in this condition increases its inherent nonlinearity. Conventional pre-emphasis techniques cannot compensate for this effect because they have a linear response. To overcome this limitation, a nonlinear equalization scheme is proposed. A dynamic VCSEL modelling technique is used to generate the time-domain optical responses for "one" and "zero" bits. Based on the asymmetry of the two responses, the rising and falling edges are equalized separately. Additionally, instead of using fixed bit delays, the equalization delay is selected based on the bias current of the VCSEL. The efficiency of the proposed modelling and equalization technique is evaluated through simulations and measurements. The transmitter achieves energy efficiency of 0.77 pJ/b at 20 Gb/s and occupies 100 μm × 60 μm active silicon area.**

***Index Terms*—Equalization, modelling, nonlinear, optical, transmitter, vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

INCREASING bandwidth requirements have pushed the traditionally electrical wireline interconnects within computing systems and data centers to their limits. As data-rates scale, the shortcomings of electrical channels are becoming more severe. Technology scaling favors I/O circuit performance, but the bandwidth of electrical channels does not scale with the same trend. Several receiver and transmitter equalization techniques [1]–[3] have been proposed to overcome this bandwidth limitation. However, these compensation techniques consume considerable power and die area, and, as a result, current high-speed I/O link designs are increasingly becoming power and channel-limited.

A possible solution to this I/O bandwidth problem is the use of optical interconnects. Optical channels, unlike their electrical counterparts, have negligible frequency-dependent loss. This provides the opportunity for optical link designs to fully utilize higher data-rates available through CMOS technology scaling, without excessive equalization complexity. However, ubiquitous acceptance of optical interconnects over the established electrical links requires them to have competitive energy- and area-efficiency metrics. Thus, in order to achieve the potential link performance advantages, emphasis must be placed on using low-power interface circuits at the transmitter and the receiver ends.

Future high-performance computing systems and networks require sub-pJ/b power efficiencies at high data-rates [4]. Fig. 1 shows the power efficiencies of the latest high-speed optical receiver and transmitter designs. Recent works in optical receivers show great potential with power efficiencies reaching as low as 0.15 pJ/b [5]–[7]. However, efficiency of VCSEL [Fig. 2(a)] based optical transmitters are mostly over 1 pJ/b [8]–[11]. One of the reasons for high power consumption in VCSEL based transmitters is their inherent bandwidth limitation. As shown in Fig. 2(b), the bandwidth of VCSEL increases as the bias current is increased. Hence they need to be driven at a high bias current to increase their effective bandwidth [12]. As data-rates scale, designers have employed pre-emphasis techniques using FIR filters to compensate for VCSEL bandwidth constraints and to allow lower bias currents [9], [10]. However, at low bias currents VCSELs are highly nonlinear and such linear FIR filters are not optimal. For linear FIR filters to be effective, VCSEL needs to be in the linear regime with high bias current and low extinction ratio (ER).

A previous work [8] incorporating nonlinear equalization has been limited to low data-rates (10 Gb/s) without significant improvement in power efficiency. The work in [13] implements a nonlinear analog equalization technique at 20 Gb/s but consumes 3.5 pJ/b. In order to design a more power-efficient equalization technique, we build a dynamic VCSEL model that takes the nonlinearity of the VCSEL into account. We use the insights from the model to propose an efficient nonlinear equalization scheme. The efficacy of the proposed technique is evaluated through simulations as well as measurements. The prototype transmitter with this equalization technique achieves energy efficiency of 0.77 pJ/b at 20 Gb/s.

This paper is organized as follows. Section II reviews the source of VCSEL nonlinearity. Section III describes the proposed VCSEL modelling technique. A new VCSEL equalization methodology that takes into account the inherent nonlinearity of the VCSEL is presented in Section IV. Section IV also discusses the simulated improvement based on the equalization technique. The circuit implementation for the VCSEL transmitter is presented in Section V. Hardware measurement results for the optical transmitter are presented in Section VI. Finally, Section VII summarizes the work by presenting the conclusions.

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M. Raj is with the California Institute of Technology, San Jose, CA 95123 USA (e-mail: makk@caltech.edu).

M. Monge and A. Emami are with the California Institute of Technology, Pasadena, CA 91125 USA.

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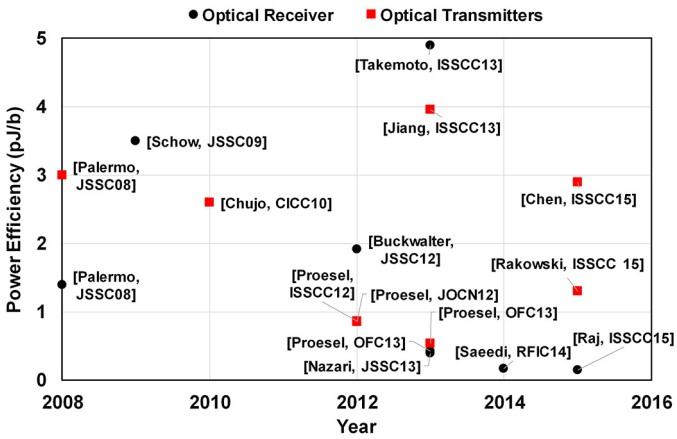


Fig. 1. Optical transceivers' power efficiency (12.5–32 Gb/s).

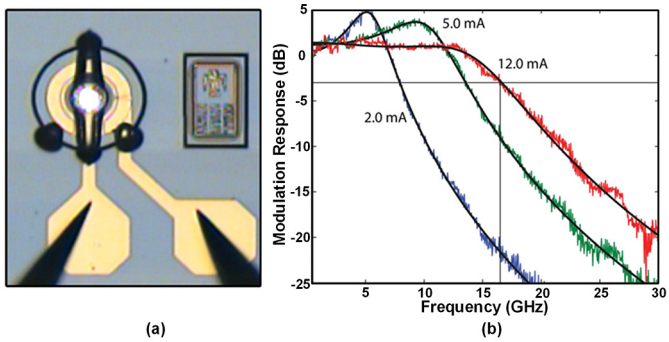


Fig. 2. (a) Die micrograph of a VCSEL. (b) Modulation response of a VCSEL at different bias currents [12].

II. VCSEL Nonlinearity

In order to simulate and optimize the VCSEL driver, we need to derive an accurate VCSEL model that includes the nonlinearity of the device. In this section we briefly review and analyze the nonlinearity of VCSEL.

VCSEL optical response depends on the interaction between electron density N and the photon density $\mathrm{N_p}$, in the laser cavity volume V. This interaction is described by two coupled differential equations [14]. The electron density increases as more carriers are injected through the device current ($\mathrm{I_{VCSEL}}$) and decreases as a number of these carriers are lost via desired stimulated and nondesired spontaneous and non-radiative recombination:

$$\frac{dN}{dt} = \frac{I_{\mathrm{VCSEL}}}{qV} - \frac{N}{\tau_{sp}} - GNN_p \tag{1}$$

where G is the stimulated emission coefficient and τ_{sp} is the nonradiative and spontaneous emission lifetime. Photon density increases as more photons are generated by stimulated and spontaneous emission and decreases as a number of them are lost due to optical absorption and scattering:

$$\frac{dN_p}{dt} = GNN_p + \beta_{sp}\frac{N}{\tau_{sp}} - \frac{N_p}{\tau_{sp}} \tag{2}$$

where τ_{p} is the photon lifetime and β_{sp} is the spontaneous emission coefficient. Combining (1) and (2) and performing the Laplace transform yields the following second-order low-pass transfer function of optical power $\mathrm{P_{opt}}$ for a given input current [14]:

$$\frac{P_{\mathrm{opt}}(s)}{I_{\mathrm{VCSEL}}(s)} = \frac{h\nu v_g \alpha_m}{q} \times \frac{GN_p}{s^2 + s\left(GN_p + \frac{1}{\tau_{sp}}\right) + \frac{GN_p}{\tau_p}} \tag{3}$$

where v_g is the light group velocity and α_m is the VCSEL mirror loss coefficient.

Rewriting (3) in terms of empirical parameters and defining $H(f) = P_{\mathrm{opt}}(f)/I_{\mathrm{VCSEL}}(f)$, we have

$$H(f) = const \times \frac{f_r^2}{f_r^2 - f^2 + j\left(\frac{f}{2\pi}\right)\gamma}. \tag{4}$$

Equation (4) is a second-order low-pass transfer function with peaking. The VCSEL relaxation oscillation/resonance frequency $\mathrm{f_r}$, which is related to the effective bandwidth, is equal to

$$f_r = \frac{1}{2\pi}\sqrt{\frac{GN_p}{\tau_p}}. \tag{5}$$

The photon density (N_p) is directly proportional to the amount of injected current above threshold [14], thus

$$f_r = D\sqrt{I_{\mathrm{VCSEL}} - I_{\mathrm{th}}} \tag{6}$$

where I_{th} is the threshold current, and D (also called D-factor) denotes the rate at which the resonance frequency increases with I_{VCSEL}. γ is the damping factor. It is proportional to the square of the resonance frequency [14] as follows:

$$\gamma = Kf_r^2 + \gamma_o. \tag{7}$$

It is clear from (6) that increasing the VCSEL current improves its resonance frequency. However, it also leads to a corresponding increase in the damping factor (7). This suggests that VCSEL modulation bandwidth cannot be increased indefinitely by increasing the bias current, as it is eventually limited by the damping factor [9]. Dependence of resonance frequency and damping factor on the bias current makes the effective frequency response of the VCSEL nonlinear when used for data modulation. Due to large change in I between the zero (I_0) and one (I_1) values (of data), the small signal assumption breaks down and the bandwidth of the VCSEL instead of being fixed, varies according to the data sequence. Thus,the VCSEL ceases to be a linear time invariant (LTI) system.

In addition to the VCSELs inherent speed limitations, another bandwidth restriction comes from the electrical parasitics of the VCSEL. The capacitance associated with the VCSEL diode, in combination with the series resistance of the distributed Bragg reflector (DBR), forms a first-order low-pass *RC* filter. At high frequencies, part of the VCSEL current is shunted outside the active region, through the parasitic capacitor, thereby hampering the effective VCSEL bandwidth. This electrical limitation is mostly linear [12].

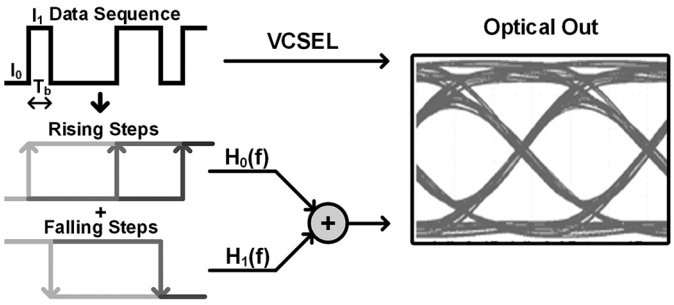


Fig. 3. Simplified, nonlinear VCSEL modeling.

III. VCSEL Modelling

An intuitive (but not exact) approach to understanding the effect of nonlinearity in the VCSEL response is shown in Fig. 3. Suppose the VCSEL is modulated with a data sequence with I_0 and I_1 being the bias currents at the zero and one levels, respectively. We also assume that rising and falling edges of the data sequence are infinitely fast. In this case, due to the finite response time of the VCSEL each rising edge will "see" a modulation response ($H_0(f)$) given by (4) with I set to I_0. Similarly, each falling edge will see a modulation response ($H_1(f)$) given by (4) with I set to I_1. With this assumption the response for the rising step ($R(t)$) and falling steps ($F(t)$) can be calculated. The incoming data stream ($D(t)$) can be expressed in terms of the summation of the rising $R(t)$ and falling $F(t)$ steps separated in time:

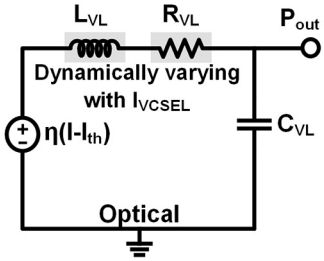
$$D(t) = \sum B(n)R\left(t - nT_b\right) + \left(1 - B(n)\right)F\left(t - nT_b\right) \quad (8)$$

where $B(n)$ represents the value of the nth t (0 or 1) and T_b is the bit period. Assuming the response of $R(t)$ is $R^*(t)$ and that of $F(t)$ is $F^*(t)$, the total VCSEL response to the input data sequence $D(t)$ can be calculated simply as

$$D^*(t) = \sum B(n)R^*\left(t - nT_b\right) + \left(1 - B(n)\right)F^*\left(t - nT_b\right). \quad (9)$$

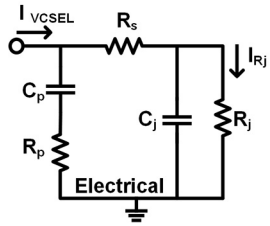
This simplified approach, although intuitive, is not practical as actual data sequences have finite rise and fall times and the assumption of infinite slope does not hold.

In order to aid the design process, exact modelling of the nonlinearity of the VCSEL's response is essential. Previous approaches have used the small signal assumption in which the modulation response for a particular bias current is used for both ones and zeroes [9]. However, this linearization leads to inaccuracies for large extinction ratios. At the other end of the spectrum, exact rate equation based VCSEL modelling, although accurate, is difficult to simulate in a circuit simulator [15]. The added complexity of rate equation based VCSEL model leads to solution convergence issues when used for transient simulations. A dynamic model based on (4)–(7), which takes into account the variation in bias current, proves to be the most efficient. For accurate modelling of VCSEL characteristics, we separate the intrinsic optical dynamics and extrinsic electrical parasitics.



Parameter	Value
Threshold current (I_{th})	0.6mA
Slope efficiency (η)	0.78mW/mA
D-factor (D)	7.6GHz/mA$^{0.5}$
K-factor (K)	0.25ns
Damping factor offset (γ_o)	37ns^{-1}

Fig. 4. VCSEL optical model.



Parameter	Value
Junction Capacitance (C_j)	110-117fF
Junction Resistance (R_j)	180-150Ω
DBR Resistance (R_s)	50Ω
Pad Capacitance (C_p)	10fF
Pad Resistance (R_p)	1Ω

Fig. 5. Electrical model of a VCSEL.

A. Optical Model

The second-order nature of the VCSEL optical dynamics (4) allows us to model them as a series RLC circuit. However, unlike [9], we make our model dynamic such that it takes into account the nonlinearity inherent in (6) and (7). Fig. 4 shows the proposed optical model. It consists of a series RLC ($R_{\rm VL}$, $L_{\rm VL}$ and $C_{\rm VL}$) circuit driven by voltage source of value $\eta(I - I_{\rm th})$. η represents the slope efficiency and $I_{\rm th}$ is the threshold current of the VCSEL. The voltage of the capacitor ($C_{\rm VL}$) is used as the output ($P_{\rm out}$). The transfer function from the voltage source to the output can be easily calculated (Fig. 4) as

$$\frac{P_{\rm out}(f)}{\eta\left(I - I_{\rm th}\right)(f)} = \frac{1}{1 - L_{\rm VL}C_{VL}\left(\frac{f}{2\pi}\right)^2 + j\left(\frac{f}{2\pi}\right)RC}. \quad (10)$$

Equation (4) has two independent variables and (10) has three, so we (arbitrarily) fix the value of $C_{\rm VL}$ to 100 fF and calculate the values of $L_{\rm VL}$ and $R_{\rm VL}$ based on (4)–(7). $L_{\rm VL}$ and $R_{\rm VL}$ can be shown to be equal to $1/4\pi^2 C_{VL}D^2(I - I_{\rm th})$ and $(\mathrm{Kf}_r^2 + \gamma_0)L_{\rm VL}$, respectively. As expected, the values of $L_{\rm VL}$ and $\mathrm{R_{VL}}$ are dependent on the bias current flowing through the VCSEL. This takes into account the inherent nonlinearity of the VCSEL. VerilogA based dynamic models of $L_{\rm VL}$ and $R_{\rm VL}$ are used in the simulation. The values of the constants in the expressions of $L_{\rm VL}$ and $R_{\rm VL}$, are also shown in Fig. 4. They are chosen to best fit the measured results in [12].

B. Electrical Model

The electrical parasitics are taken into account using the conventional approach used in [9]. Fig. 5 shows the electrical model of the VCSEL. $C_{\rm j}$ and $R_{\rm j}$ represent the junction capacitance and resistance, respectively. The series resistance of the DBR mirrors is represented by R_s in Fig. 5. C_p and R_p represent the pad capacitance and resistance. In Fig. 5, a part of the total current ($I_{\rm VCSEL}$) gets diverted to the parasitic capacitors

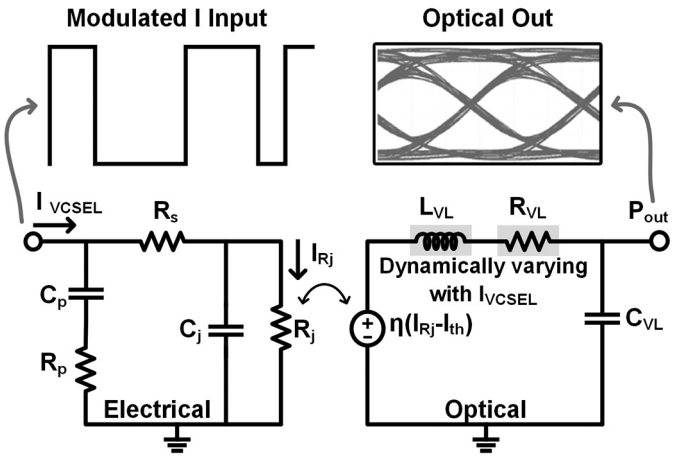


Fig. 6. Complete dynamic VCSEL model.

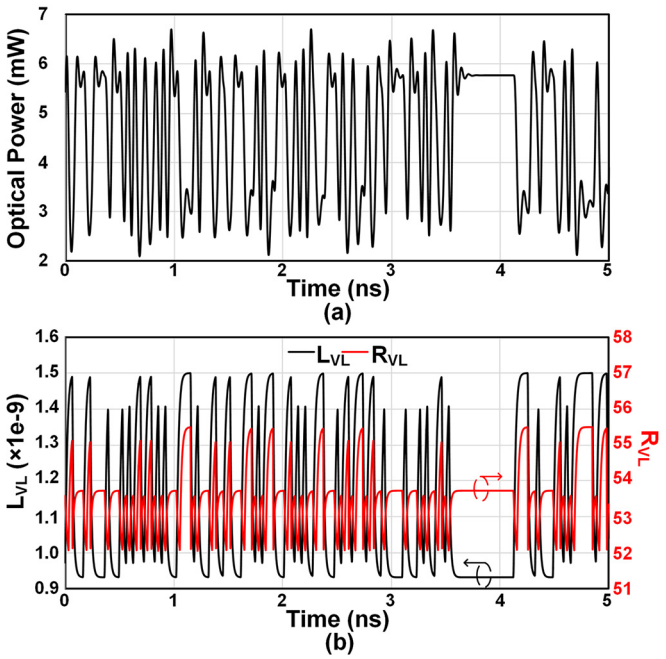


Fig. 7. Transient simulation based on VCSEL model showing (a) VCSEL power and (b) variation in L_{VL} and R_{VL}.

C_j and C_p, which form a low impedance path at high frequencies. The actual amount of current available for electrical to optical conversion, is represented by the current flowing into the junction resistance (I_{Rj}). The electrical model parameters have been summarized in Fig. 5. They are chosen to best fit the measured results in [12].

C. Complete Model

The complete dynamic model of the VCSEL is shown in Fig. 6. The electrical and optical models are combined by changing the voltage source of the optical model to a current dependent voltage source of value $\eta(I_{\mathrm{Rj}} - I_{\mathrm{th}})$. $\mathrm{I_{Rj}}$ is the current flowing through the junction resistance. To use this model in a circuit simulator, the modulated current is provided to the input of the electrical model and the output of the optical part generates the effective optical power (P_{out}). Modelled in VerilogA, the values of L_{VL} and R_{VL} are updated at each simulation time-step. Thus, L_{VL} and R_{VL} track the changes VCSEL output (Fig. 7) and remain constant during a long sequence of "1" or "0" and changing rapidly during "1010" transitions.

To evaluate the accuracy of our VCSEL modelling, we generated the modulation response (H(f)) for different bias currents and compared it against the measured modulation response from [12]. As shown in Fig. 8, the simulated modulation response matches closely with the shape and bandwidth of the measured response for different bias currents. For example, the measured bandwidth for an 11.5 mA bias current is 20 GHz and that predicted by the model is 19.89 GHz. In addition, the measured results in [12] suggest that the maximum bandwidth is achieved at 11.5 mA and then bandwidth diminishes as current increases. To verify whether the model also predicts the same, we plotted the bandwidth based on simulation of the model for different bias currents. As shown in Fig. 9, the bandwidth reaches a maximum of 19.89 GHz at 11.5 mA and then decreases as current is increased further.

IV. VCSEL Equalization Methodology

Bandwidth limitations in the VCSEL's optical response limits the speed of optical transmitters. In addition, better power efficiency and mean time to failure (MTTF) [16] demands the biasing of the current at a lower bias current and thus, lower bandwidth. As data-rates scale, there is an increased need to have equalization circuitry to compensate for the VCSEL bandwidth restrictions. Previous designs have mostly relied on established electrical transmitter equalization techniques [9], for example, finite impulse response (FIR)-based pre-emphasis. Conventional pre-emphasis technique is designed to efficiently equalize linear time-invariant channels. However, a VCSEL does not have a linear frequency response.

Fig. 10(a) and (b) show the responses of isolated one and zero pulses generated from our model. The I_0 and I_1 are set to 4 mA and 9 mA, respectively. The responses are superimposed after flipping the zero response in Fig. 11(a). As expected, due to the nonlinearity of the VCSEL, the two responses are not equal. The asymmetry becomes more pronounced as the bias current is reduced. Fig. 11(b), shows the pulse responses for an isolated one and an isolated zero with reduced I_0 (2 mA) and I_1 (4.5 mA) but the same ER. For the same ER, there is greater difference between the one and the zero responses for the lower current case. The conventional FIR based transmitter equalization would be "blind" to this asymmetry, i.e. it would equalize an isolated one pulse in the same manner as the isolated zero, leading to suboptimal performance.

The fundamental cause of the asymmetry between isolated one and zero responses is that the nonlinearity in the VCSEL causes it to respond differently to rising and falling edges of data. To take this effect into account, we detect the rising and falling edges and equalize them differently, based on the response of the VCSEL to an isolated zero and isolated one. Fig. 12 shows the architecture of the proposed equalization technique. Input data (D_{in}) is delayed by an equalization delay of t_{eq}. Unlike conventional digital FIR-transmitter

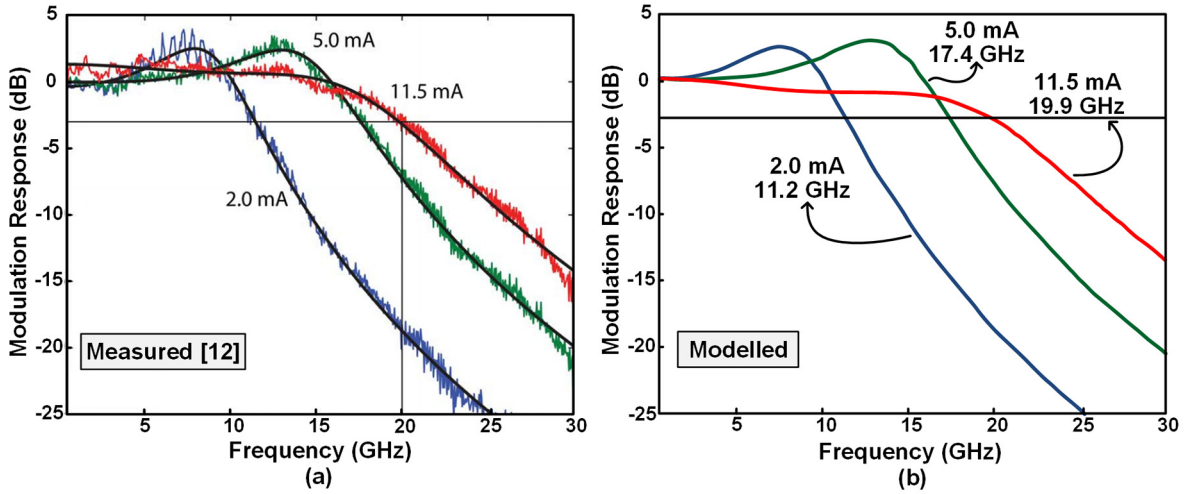


Fig. 8. VCSEL modelling: comparing the (a) measured with (b) simulated.

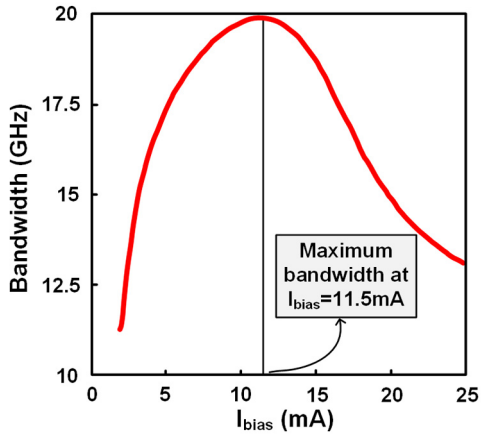


Fig. 9. Simulated modulation bandwidth variation with bias current.

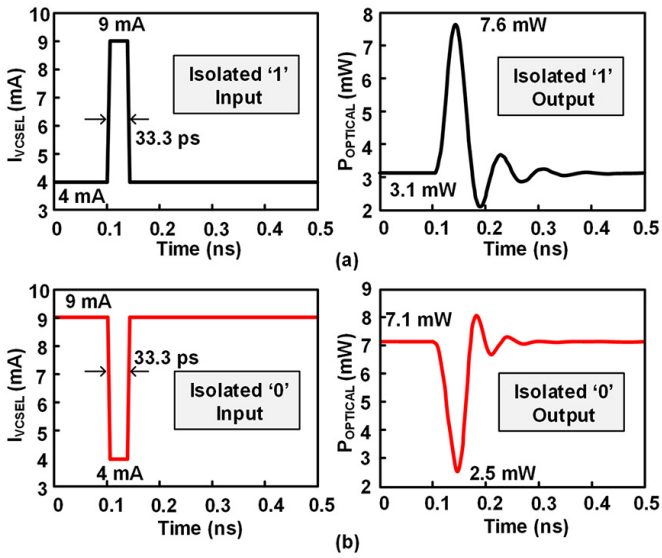


Fig. 10. VCSEL pulse response for (a) isolated 1 and (b) isolated 0.

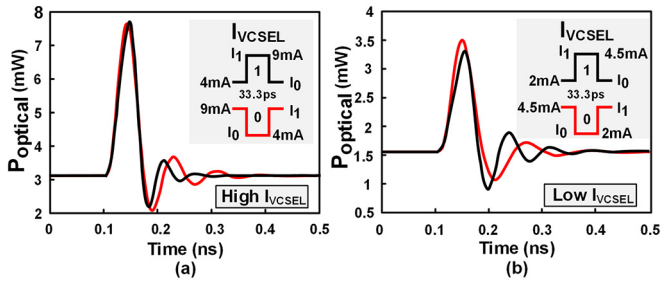


Fig. 11. VCSEL pulse responses for (a) high and (b) low I_{VCSEL}.

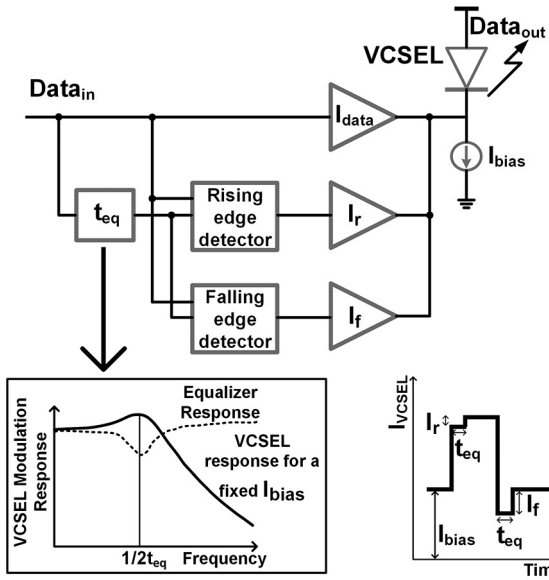


Fig. 12. Proposed equalization technique.

pre-emphasis, the t_{eq} is not set to be a multiple of the bit period. Simulations based on the VCSEL model show that the effect of the proposed equalization technique is to cancel the peaking in the typical second order response of the VCSEL. The minimum of this "anti-peak" occurs at $1/2t_{\mathrm{eq}}$. Thus, we set the

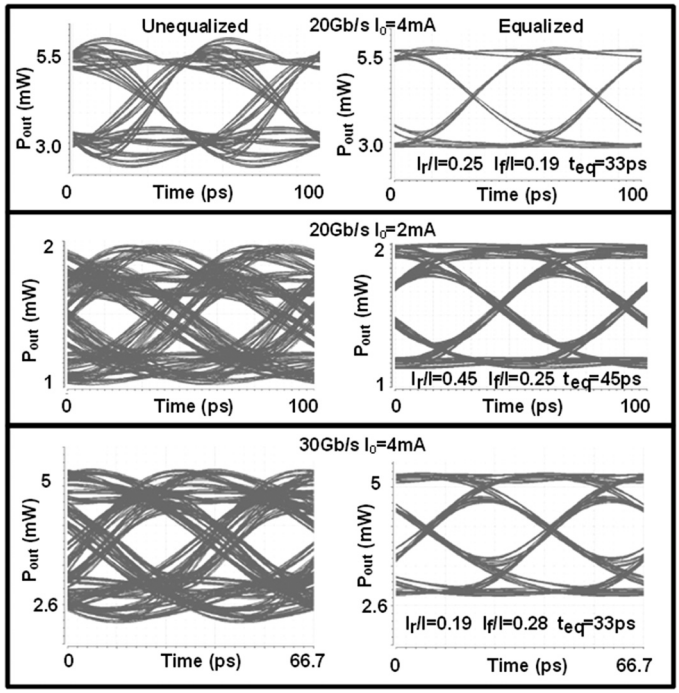


Fig. 13. Simulated optical eye-diagrams for PRBS-15 data with and without equalization.

TABLE I
SUMMARY OF SIMULATED IMPROVEMENT BY THE PROPOSED VCSEL EQUALIZATION TECHNIQUE

Data-Rate	I_{bias}	Rise Tap (I_r/I)	Fall Tap (I_f/I)	t_{eq}	% vertical improvement	% horizontal improvement
20 Gb/s	4mA	0.25	0.19	33ps	16%	22%
20 Gb/s	2mA	0.45	0.25	45ps	70%	38%
30 Gb/s	4mA	0.19	0.28	33ps	10%	33%

$t_{\rm eq}$ based on the position of the peak of the VCSEL's modulation response. This response itself is dependent on the bias current independent of the data-rate.

To investigate the efficacy of the proposed equalization technique, we performed two sets of simulations to generate optical eye-diagrams using the VCSEL model (for a PRBS-15 data sequence). In the first case no equalization was used and in the second case we used the proposed technique. Fig. 13(a) and (b) show the simulated eye-diagram for 20 Gb/s with the VCSEL biased at ($I_{\rm bias}$) 4 mA and 2 mA respectively. Fig. 13(c) shows the simulated eye-diagrams for 30 Gb/s with an $I_{\rm bias}$ of 4 mA. The extinction ratio was fixed to 2 dB for all three cases. The percentage improvement in the vertical and horizontal eye opening and the required tap strengths (I_r/I and I_f/I) and $t_{\rm eq}$ are presented in Table I. Three important facts are suggested by Table I. First, for efficient VCSEL equalization the rise and fall taps must be asymmetric. Secondly, the proposed technique is more effective when the VCSEL is biased at a low current. Finally, the $t_{\rm eq}$ delay is independent of the data-rate and is dependent on the bias current ($I_{\rm bias}$). We also compared the proposed technique with conventional FFE by making rising (I_r/I) and falling (I_f/I) taps the same. Fig. 14 compares optimally equalized 20Gb/s eye with $I_r/I = 0.45$ and $I_f/I = 0.25$ with conventional FFE with $I_r/I = I_f/I = 0.35$. The proposed approach improves the vertical and horizontal eye opening by 26.3% and 7.7% respectively.

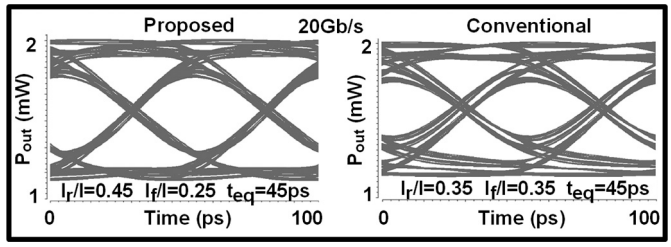


Fig. 14. Simulated eye diagrams based on proposed and conventional (FFE) equalization.

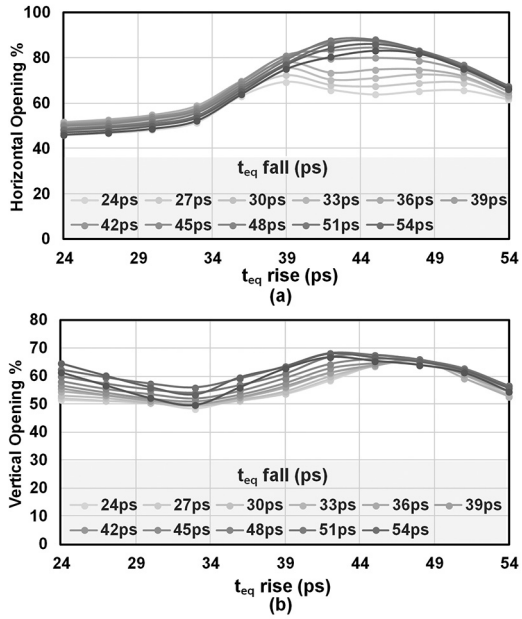


Fig. 15. Simulated effect of different $t_{\rm eq}$ rise and $t_{\rm eq}$ fall on (a) horizontal and (b) vertical eye opening at 20 Gb/s.

We also investigated the advantage of having different $t_{\rm eq}$ for the rising and falling edges, similar to [8]. Fig. 15 shows the vertical and horizontal eye openings at 20Gb/s with an $I_{\rm bias}$ of 2 mA, for different $t_{\rm eq}$ for rising and falling edges. The $t_{\rm eq}$ rise and $t_{\rm eq}$ fall were varied from 24 to 54 ps in steps of 3 ps with rise tap (0.45) and fall tap (0.25) values fixed. Fig. 15 shows that horizontal eye opening is more sensitive to $t_{\rm eq}$ than vertical eye opening. The optimum horizontal opening of 88% was obtained for $t_{\rm eq}$ rise $= 45$ ps and $t_{\rm eq}$ fall $= 45$ ps and optimum vertical opening of 67% occurs for $t_{\rm eq}$ rise $= 42$ ps and $t_{\rm eq}$ fall $= 48$ ps. The optimum vertical opening for when $t_{\rm eq}$ rise $= t_{\rm eq}$ fall $= 45$ ps is only 0.7% worse. Thus, different $t_{\rm eq}$ for rising and falling edges has minimal improvement on eye opening but it does require having a second delay line and thus additional power dissipation. Hence, $t_{\rm eq}$ was kept the same for both rising and falling edges in our design.

V. CIRCUIT IMPLEMENTATION

Fig. 16 shows the circuit architecture of the proposed VCSEL equalization scheme. In order to generate a (pseudo) random bit

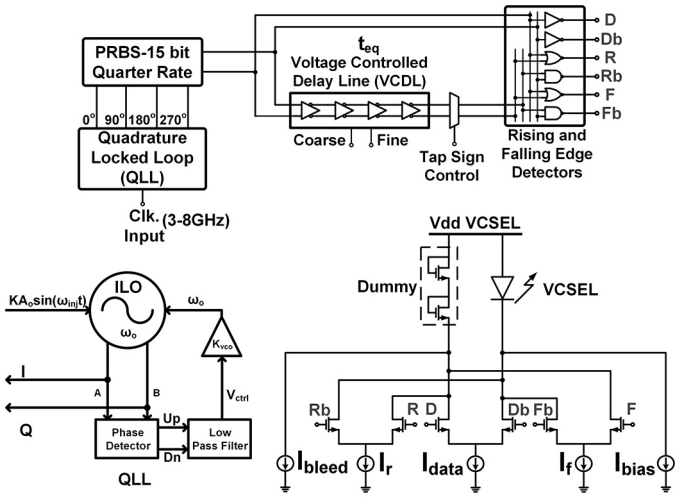


Fig. 16. Circuit architecture.

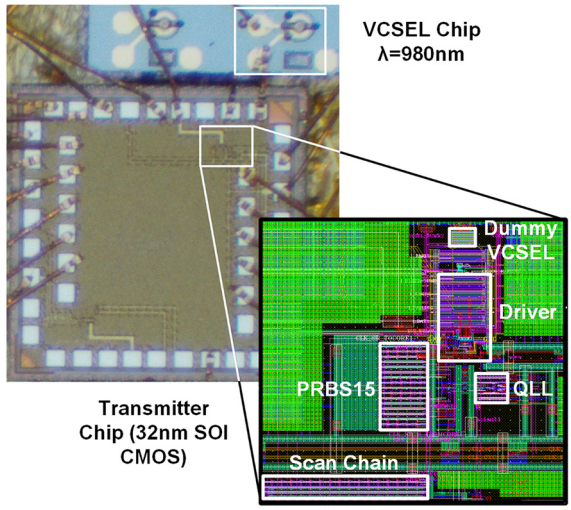


Fig. 17. Chip micrograph and layout details.

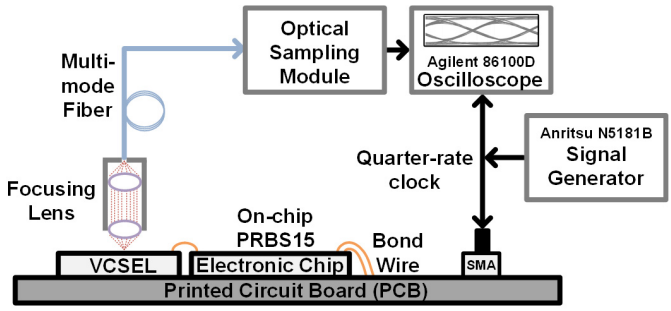


Fig. 18. Measurement setup.

sequence, an on-chip high-speed quarter-rate PRBS-15 transmitter is used. Quarter-rate architecture is chosen to relieve the speed requirement of the PRBS generator. A quadrature locked loop (QLL) [5] based front-end is used for converting the low swing input clock (∼100 mV) to the rail-to-rail digital domain. It consists of an injection locked 2 stage differential ring oscillator with quadrature outputs. A quadrature error tracking loop consisting of a XOR gate based phase detector, charge pump and a low pass filter is used to maintain quadrature accuracy as well as to ensure large locking range (3–8 GHz). The QLL enables the generation of accurate quadrature phase clocks for the quarter-rate PRBS, from single phase of clock. Conventional clock front-ends use power-hungry CML-to-CMOS convertors. In contrast, the QLL based clocking uses the inherent high voltage gain of injection locking [17] to generate rail-to-rail clock from the low amplitude analog clock input at a low power overhead.

The equalization delay ($t_{\rm eq}$) is implemented by a four stage differential delay stage with varactors based analog and 2 bit digital delay controls for fine and coarse delay adjustments. It has a total delay range of 25 ps to 45 ps. To make our design more power efficient and scalable with technology, the rising and falling edge detectors are implemented via digital CMOS gates. A typical VCSEL output driver, with a differential stage steering current between the VCSEL and a dummy load, and an additional static current source ($I_{\rm bias}$), to bias the VCSEL sufficiently above the threshold current, is used. The rise and fall taps are implemented by adding additional differential pairs to the output driver. The tail current sources for all the differential pairs are implemented using the low voltage cascode structure. The tail currents are controlled externally to control the strength of the taps. The output stage is designed for a higher voltage supply (2.5 V) due to the typical VCSEL diode knee voltage (1.7 V) exceeding normal CMOS supplies (1 V).

VI. Measurement Results

The prototype was fabricated in a 32 nm SOI CMOS process. The die micrograph and layout details are presented in Fig. 17. Core area is 100 μm × 60 μm, in a 1 mm × 1 mm die. The VCSEL has a wavelength of 980 nm and is wire-bonded to the transmitter chip. Fig. 18 shows the measurement setup. An external Anritsu N5181B clock generator is used to supply a single phase clock to the QLL frontend. The QLL frontend is used to generate the quadrature phase clocks for the high-speed quarter-rate PRBS-15 generator. The quarter-rate PRBS generator was measured to operate in the range of 15–32 Gb/s. The optical output from the VCSEL is focused on multi-mode fiber (MMF) which connects to an Agilent 86100D oscilloscope with an optical sampling module for data eye measurements.

A. Optical Measurement Setup

An essential part of the optical measurement setup is coupling the light from the VCSEL to the optical fiber. Light can be simply coupled by appropriately positioning a cleaved bare optical fiber near the surface of the VCSEL (butt coupling). However, due to the divergence angle out of the VCSEL being larger than the acceptance angle into the fiber, there is a loss of about −3 dB. In addition, vibrations (due to air) in the bare fiber translates to optical noise. Fig. 19 shows the setup for bare fiber coupling.

Instead of butt coupling the measurement setup shown in Fig. 20 is used. The setup relays the image of the VCSEL onto the surface of the fiber, with the magnification of 2×. The 4 μm diameter VCSEL spot gets imaged to an 8 μm diameter at the

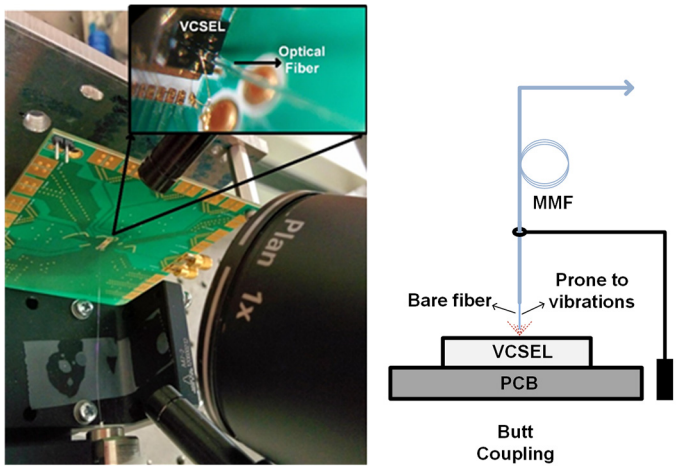


Fig. 19. Butt coupling proves too lossy and noisy for VCSEL measurements.

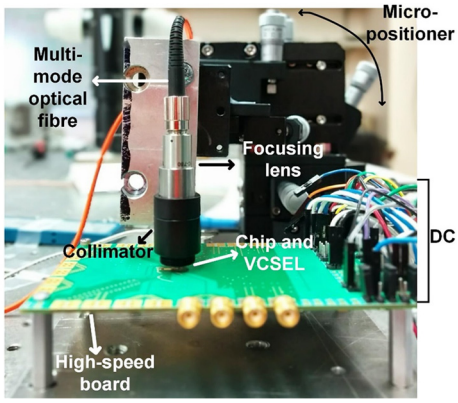


Fig. 20. Optical measurement setup.

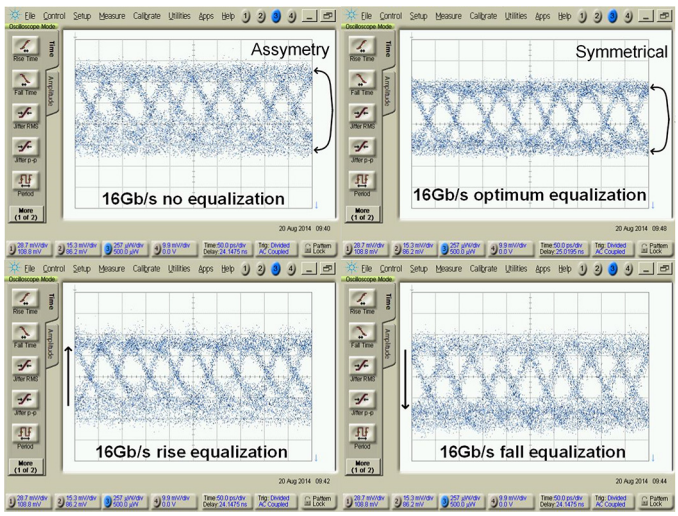


Fig. 21. Measured VCSEL optical output at 16 Gb/s (PRBS-15), with and without equalization.

surface of the fiber, while at the same time the divergence angle going into the fiber is divided by two relative to the divergence angle directly out of the VCSEL, leading to more efficient coupling. Two lenses with a ratio of two in focal lengths are used to achieve this. A 6 mm lens is used to collimate the light coming

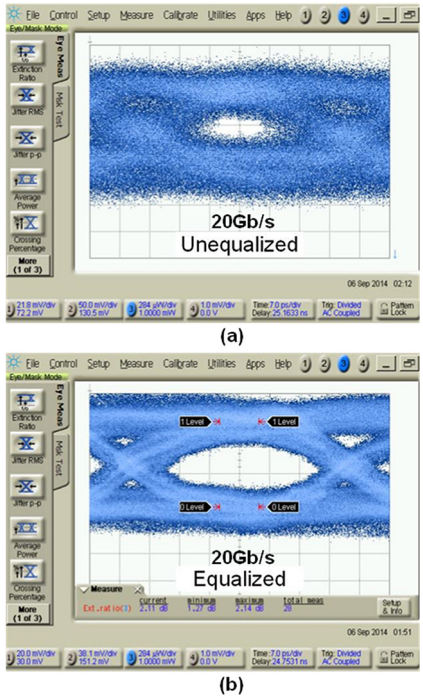


Fig. 22. Measured optical eye-diagram for PRBS-15 data at 20 Gb/s. (a) Unequalized. (b) Equalized.

from the VCSEL and an 11 mm lens is used to focus the collimated light into the fiber. An angle-polished multi-mode fiber is connected to the lens setup via a standard APC connector. The fiber is polished at an 8° angle to avoid optical feedback. This setup helped in reducing the coupling loss to -0.5 dB.

B. Measured Eye-Diagrams

In order to establish the efficacy of the proposed equalization technique, VCSEL outputs were measured for four cases at a data-rate of 16 Gb/s at low current bias (I_{bias}). As shown in Fig. 21, without any equalization the eye is open but there is an asymmetry of the one and zero levels. The optical noise is greater for the zero level than for the one level. The rise tap proves more effective in countering this asymmetry than the fall tap. The optimum symmetrical eye is achieved when the rise and fall taps have a ratio of 2:1. The t_{eq} was set to its maximum value (45 ps). Average optical DC power was fixed at 1.5 mW for all four measurements.

At 20 Gb/s, without equalization, the measured data eye-diagram [Fig. 22(a)] shows 1.2 dB ER and 35% horizontal opening. With equalization [Fig. 22(b)], the output optical eye improves to 65% horizontal opening, ER of 2.1 dB and optical modulation amplitude (OMA) of 0.9 dBm. The ratio of the rise and fall taps is again 2:1. Both differential and single-ended operations of the output stage are verified. The VCSEL output stage in single-ended mode draws 5.5 mA from a 2.5 V power supply. The rest of the equalization circuitry (excluding the QLL and PRBS15 generator) consumes 1.6 mA from a 1 V supply. This translates to an efficiency of 0.77 pJ/b. The maximum data-rate of 20 Gb/s is limited by the bandwidth of the VCSEL and its modal noise [18]. Performance summary and

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work	JSSC 08 [9]	MTT 10 [8]	ISSCC 13 [10]	ISSCC 14 [11]	ISSCC 12 [20]	OFC 13 [19]	JOCN 12 [21]
Technology	**CMOS SOI 32nm**	CMOS 90nm	CMOS 90nm	CMOS 65nm	SiGe 0.13μm	CMOS 90nm	CMOS SOI 32nm	CMOS 90nm
Supply (V)	**1.0/2.5**	1.0/2.8	1.0/-	1.2/3.6	2.5/3.3	1.0/2.2	0.63/ 2.25	0.63/ 2.25
Data-Rate (Gb/s)	**20**	16	10	25	40	17.5	25	22.5
Power (pJ/b)	**0.77**	3.0	5.0	3.96	7.80	0.87	0.54	0.85
OMA(dBm)	**0.9**	1.4	2.5	0.8	2.3	-1.1	-	-0.4
Equalization Technique	**Assym. FFE**	FFE	Assym. FFE	FFE	FFE*	None	None	FFE

* With group delay compensation

comparison are presented in Table II. We achieve a competitive OMA at a power efficiency second only to [19], which uses a lower supply voltage for the driver circuitry (0.63 V) and the VCSEL itself (2.25 V).

VII. CONCLUSION

There exists a fundamental tradeoff between power efficiency and bandwidth of a VCSEL. Driving the VCSEL at a low bias current boosts power efficiency but makes it more nonlinear, thus making conventional pre-emphasis inefficient. To break this trade-off a novel VCSEL modeling and an efficient equalization technique that takes into account the inherent nonlinearity in the VCSEL's frequency response are presented. The time domain optical responses based on the dynamic VCSEL model verify that the nonlinearity becomes more severe at low VCSEL currents. The rising and falling edges are equalized separately and the equalization delay was selected based on the bias current of the VCSEL. The equalization technique is used to achieve energy efficiency of 0.77 pJ/b at 20 Gb/s with an OMA of 0.9 dBm and 65% horizontal opening. The measured results proves the efficacy of the proposed equalization technique for ultra-low-power VCSEL based transmitter design.

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Mayank Raj (S'08) was born in Patna, India, in 1987. He received the B.Tech. degree from the Indian Institute of Technology, Kanpur, India, in 2008, and the M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, CA, USA, in 2009 and 2014, respectively, all in electrical engineering.

In 2014, he joined Xilinx Inc., San Jose, CA, USA, where he works on high-performance mixed-signal integrated circuits for high-speed and low-power interconnects. He holds six U.S. patents in the field of mixed-signal integrated circuit design.

Dr. Raj was the recipient of the 2008 California Institute of Technology Atwood Fellowship and the 2015 Intel/IBM/Catalyst Foundation CICC Student Scholarship Award.

Manuel Monge (S'09) received the B.S. degree in electrical engineering (with honors) from the Pontifical Catholic University of Peru (PUCP), Lima, Peru, in 2008, and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2010, where he is currently working towards the Ph.D. degree.

His research interests include analog and mixed-signal integrated circuits (IC), ultra-low-power systems, and the hybrid integration of ICs with novel materials and devices, with focus on biomedical and health care applications, specifically implantable, wearable and point-of-care medical devices. He spent the summer of 2013 at Samsung Display America Laboratory (SDAL) working on on-chip channel monitoring circuits for high-speed links.

Mr. Monge was the recipient of the PUCP Best Student Award in 2008, the Fulbright Peru Opportunity Grant Scholarship in 2008, and the Caltech Atwood Fellowship in 2009. He was the third place winner of the 2013 Broadcom Foundation University Research Competition and was named the 2014 Caltech Rosen Scholar.

Azita Emami (S'97–M'04) was born in Naein, Iran. She received the B.S. degree (with honors) from Sharif University of Technology, Tehran, Iran, in 1996, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1999 and 2004, respectively.

She is currently a Professor of electrical engineering with the California Institute of Technology, Pasadena, CA, USA. From July 2006 to August 2007, she was with Columbia University, New York, NY, USA, as an Assistant Professor with the Department of Electrical Engineering. She was a Research Staff Member with IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, from 2004 to 2006. Her current research areas are high-performance mixed-signal integrated circuits and VLSI systems, with focus on high-speed and low-power optical and electrical interconnects, clocking, biomedical implant and compressed sensing.