A 20Gb/s 0.77pJ/b VCSEL Transmitter with Nonlinear Equalization in 32nm SOI CMOS

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***Abstract* — This paper describes an ultra-low-power VCSEL transmitter in 32nm SOI CMOS. To increase its power efficiency, the VCSEL is driven at a low bias current. The resulting nonlinearity and loss in bandwidth is modelled and compensated by a nonlinear equalization technique. The time domain optical responses for "one" and "zero" bits are used to find the optimum equalization technique. The rising and falling edges were equalized separately and the equalization delay is selected based on the bias current of the VCSEL. The transmitter achieves energy efficiency of 0.77pJ/b at 20Gb/s.**

***Index Terms* — vertical-cavity surface-emitting laser (VCSEL), optical, nonlinear, transmitter, equalization.**

I. Introduction

As the bandwidth demand for traditionally electrical wireline interconnects has accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems and data centers. Future high-performance computing systems and networks require sub-1pJ/bit power efficiencies at high data rates [1]. Recent works in optical receivers show great potential with power efficiencies reaching as low as 0.15pJ/b [2]. However, efficiency of VCSEL based optical transmitters are still over 1pJ/b [3]-[6]. One of the reasons for high power consumption in VCSEL based transmitters is their inherent bandwidth limitation. They need to be driven at a high bias currents to increases their effective bandwidth [7].

As data-rates scale, designers have employed pre-emphasis techniques using FIR filters to compensate for VCSEL bandwidth constraints and to allow lower bias currents [4], [5]. However, at low bias currents VCSELs are highly non-linear and such linear FIR filters are not optimal. For linear FIR filters to be effective, VCSEL needs to be in the linear regime with high bias current and low extinction ratio (ER).

A previous work incorporating nonlinear equalization has been limited to low data-rates (10Gb/s) without significant improvement in power efficiency [3]. We present a dynamic VCSEL modelling approach that leads to an efficient equalization technique compensating VCSEL's inherent nonlinear response. The prototype transmitter with this equalization technique achieves energy efficiency of 0.77pJ/b at 20Gb/s.

II. VCSEL Nonlinearity

In order to simulate and optimize the VCSEL driver, we need to drive an accurate VCSEL model that includes the nonlinearity of the device. In this section we briefly describe and analyze the nonlinearity of VCSEL.

Optical bandwidth of VCSELs is regulated by two coupled differential equations which describe the interaction of the electron density and the photon density [4]. Combining the two rate equations yields the following second-order low-pass transfer function of optical power (P_{opt}) for a given input current (I_{VCSEL}), i.e. $H(f) = P_{opt}(f)/I_{VCSEL}(f)$ is given by:

$$H(f) = const \times f_r^2/(f_r^2 - f^2 + j(f/2\pi)\gamma) \quad (1)$$

f_r (resonance frequency) is the relaxation oscillation frequency and is related to the effective bandwidth [7]:

$$f_r = D\sqrt{I_{VCSEL} - I_{th}} \quad (2)$$

I_{th} is the threshold current, and D (also called D-factor) denotes the rate at which the resonance frequency increases with I_{VCSEL}. The damping factor (γ) is proportional to the square of the resonance frequency [7]:

$$\gamma = Kf_r^2 + \gamma_o \quad (3)$$

K, also called K-factor, sets the maximum intrinsic modulation bandwidth of the VCSEL, and γ_o is the damping factor offset. Dependence of resonance frequency (f_r) and damping factor (γ) on I_{VCSEL} makes the effective frequency response of the VCSEL nonlinear when used for data modulation. Due to large change in I_{VCSEL} between the zero (I_0) and one (I_1) values (NRZ data), the small signal assumption breaks down and the bandwidth of the VCSEL varies according to the data sequence. Thus the VCSEL ceases to be a linear time invariant (LTI) device.

In addition to the VCSELs inherent speed limitations another bandwidth limitation comes from the capacitance of the VCSEL, which in combination with the series resistance (dominated by the resistance of the DBRs), forms a low-pass RC filter that shunts the modulation current outside the active region at frequencies above the

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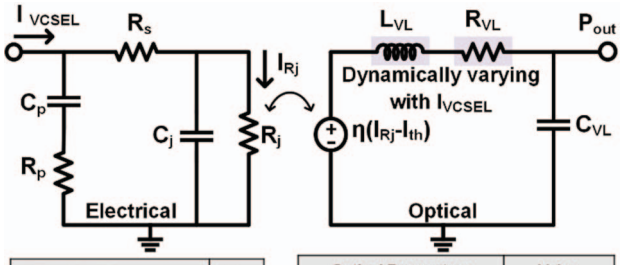

Electrical Parameters	Value
Junction Capacitance (C_j)	110fF
Junction Resistance (R_j)	150Ω
DBR Resistance (R_s)	50Ω
Pad Capacitance (C_p)	10fF
Pad Resistance (R_p)	1Ω

Optical Parameters	Value
Threshold current (I_{th})	0.6mA
Slope efficiency (η)	0.78mW/mA
D-factor (D)	7.6GHz/mA$^{0.5}$
K-factor (K)	0.25ns
Damping factor offset (γ_0)	37ns^{-1}

Fig. 1. Dynamic model a VCSEL.

bandwidth of the filter. This electrical limitation is mostly linear [7].

III. VCSEL Modelling

For accurate modelling of VCSEL characteristics, we separate the intrinsic optical dynamics and extrinsic electrical parasitics.

The second order nature of the VCSEL optical dynamics (1) allows us to model them as a series RLC circuit [4]. However, unlike [4], we make our model dynamic such that it takes into account the nonlinearity inherent in (2) and (3). Fig. 1 shows the proposed optical model consisting of a series RLC (R_{VL}, L_{VL} and C_{VL}) circuit that is driven by a dependent voltage source $\eta(I_{Rj}-I_{th})$, with η representing the slope efficiency and I_{th} the threshold current of the VCSEL. The voltage of the capacitor (C_{VL}) is used as the output (P_{out}). We (arbitrarily) fix the value of C_{VL} to 100fF and calculate the values of L_{VL} and R_{VL} based on (1-3). L_{VL} and R_{VL} can be shown to be $1/\{4\pi^2 C_{VL} D^2 (I_{Rj}-I_{th})\}$ and $(Kf_r^2+\gamma_0)L_{VL}$, respectively. As expected, the values of L_{VL} and R_{VL} are dependent on the current flowing through the VCSEL (I_{VCSEL}). This takes into account the inherent nonlinearity of the VCSEL. Verilog-A based dynamic models of L_{VL} and R_{VL} are used in the simulations.

The electrical parasitics are taken into account using the conventional approach used in [4]. C_j and R_j represent the junction capacitance and resistance, respectively. DBR resistance is represented by R_s. C_p and R_p represent the pad capacitance and resistance formed between the p-bond pad and the conducting n-side.

The complete dynamic model of the VCSEL is shown in Fig. 1. The electrical and optical models are combined by changing the voltage source of the optical model to a current dependent voltage source and replacing I_{VCSEL} with I_{Rj} (the current flowing in the junction resistance). To use this model in a circuit simulator, the modulated current is provided to the input of the electrical model and the output of the optical part generates the effective optical power (P_{out}). Model parameters have been tabulated in Fig. 1.

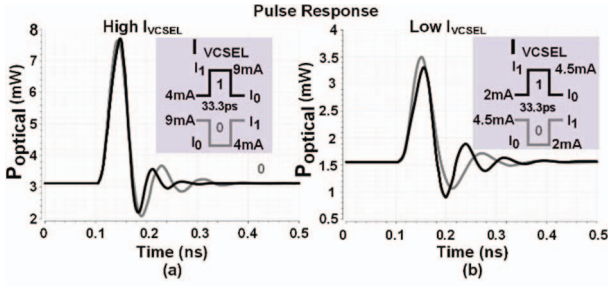

Fig. 2. VCSEL pulse responses for (a) high and (b) low I_{VCSEL}.

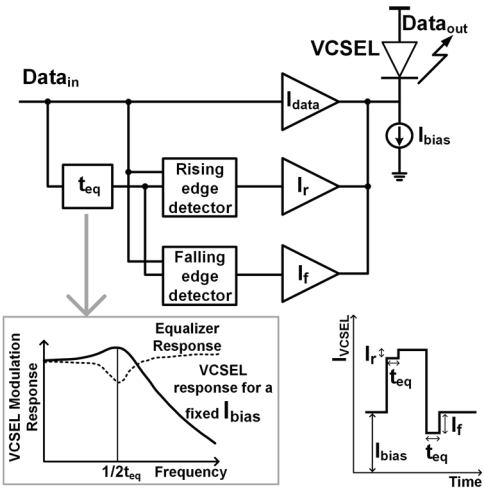

Fig. 3. Proposed equalization technique.

IV. Proposed Equalization Technique

Fig. 2(a) shows the pulse responses for an isolated one and an isolated zero based on our model. The I_0 and I_1 are set to 4mA and 9mA respectively. The responses are superimposed after flipping the zero response. As expected due to the nonlinearity of the VCSEL, the two responses are not equal. The asymmetry becomes more pronounced as the bias current is reduced. Fig. 2(b), shows the pulse responses for an isolated one and an isolated zero with reduced I_0 (2mA) and I_1 (4.5mA) but the same extinction ratio (ER). It is clear that there is a greater difference between the one and the zero responses. The conventional FIR based transmitter equalization would be "blind" to this asymmetry, i.e. it would equalize an isolated one pulse in the same manner as the isolated zero, leading to sub-optimal performance.

To take the nonlinear behavior of VCSEL into account it is necessary to modify the pre-emphasis [3]. One possible

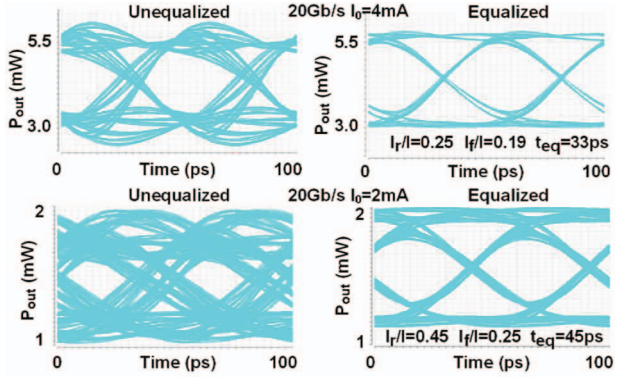

Fig. 4. Simulated optical eye-diagrams for PRBS-15 data with and without equalization.

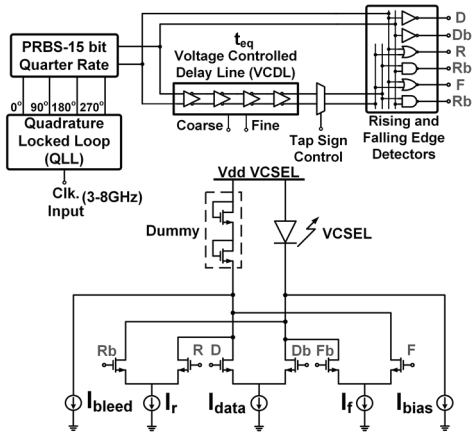

Fig. 5. Circuit architecture.

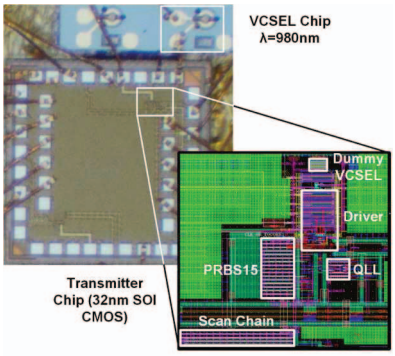

Fig. 6. Die micrograph and layout details.

approach is to detect the rising and falling edges and equalize them differently based on the response of the VCSEL to each transition. Fig. 3. shows the architecture of the proposed equalization technique. Input data (D_{in}) is delayed by an equalization delay of t_{eq}. Unlike conventional digital FIR-transmitter pre-emphasis the t_{eq} is not set to be a multiple of the bit period. Simulations based on the VCSEL model show that the effect of the proposed equalization technique is to cancel the peaking in the typical second order response of the VCSEL. The minimum of this "anti-peak" occurs at $1/2t_{eq}$. Thus, we set the t_{eq} based on the position of the peak of the VCSEL's modulation response. This response itself is dependent on the bias current and independent of the data-rate. To investigate the efficacy of the proposed equalization technique, we performed two sets of simulations to generate optical eye-diagrams using the VCSEL model. Fig. 4 shows the simulated eye-diagrams at 20Gb/s with and without equalization, for I_0=4mA and I_0=2mA. The technique is more efficient at low I_{VCSELs}.

V. Circuit Implementation

Fig. 5 shows the circuit architecture of the proposed system. An on-chip quarter-rate PRBS-15 generator is used to generate the random test data pattern. Quarter-rate architecture is chosen to relieve the speed requirement of the PRBS generator. A quadrature locked loop (QLL) [2] based front-end is used for converting the low swing input clock (~100mV) to rail-to-rail digital domain, without using conventional CML-to-CMOS convertors. The QLL also enables the generation of quadrature phase clocks for the quarter-rate PRBS circuit. The quadrature error tracking loop ensures a large locking range and accurate quadrature phase generation.

An inverter based four stage differential voltage-controlled delay line is used to generate the equalization delay (t_{eq}). It has a total delay range of 25ps to 40ps. The rising and falling edge detectors are implemented via digital CMOS logic (Fig. 5). The VCSEL output driver is a differential stage steering current between the VCSEL and a dummy load. An additional static current source is used to bias the VCSEL sufficiently above the threshold current. The rise and fall taps are added via two independent differential pairs as shown in Fig. 5. The tail current sources for all the differential pairs are implemented using the low voltage cascode structure. I_r and I_f are adjustable and used to control the strength of the taps. The output stage is designed for a higher voltage supply (2.5V) due to the typical VCSEL diode knee voltage (1.7V) exceeding normal CMOS supply voltages (1V).

VI. Measurement Results

The prototype was fabricated in a 32nm SOI CMOS process. The die micrograph and layout details are presented in Fig. 6. Core area is 100µm × 60µm, in a 1mm × 1mm die. The VCSEL has a wavelength of 980nm and is wire-bonded to the transmitter chip (Fig. 6). An external clock generator is used to supply a single phase clock to the QLL frontend. The QLL has a locking range of 3-8GHz;

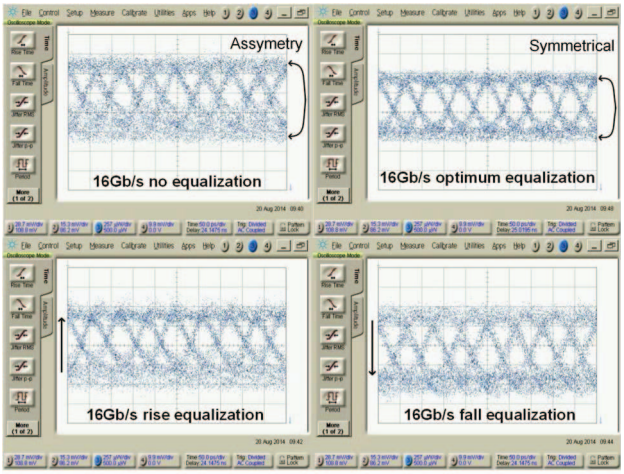

Fig. 7. Measured VCSEL optical output at 16Gb/s (PRBS-15), with and without equalization.

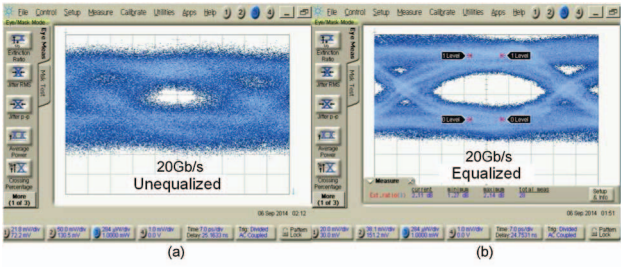

Fig. 8 Measured optical eye-diagram for PRBS-15 data at 20Gb/s. (a) Unequalized (b) Equalized.

the quarter-rate PRBS generator was measured to operate in the range of 15-32Gb/s.

In order to establish the efficacy of the proposed equalization technique, VCSEL outputs were measured for four cases at a data-rate of 16Gb/s at a low current bias. As shown in Fig. 7, without any equalization the eye is open but there is an asymmetry of the one and zero levels. The optical ISI noise is greater for the zero level than for the one level. The rise tap proves more effective in countering this asymmetry than the fall tap. The optimum symmetrical eye is achieved when the rise and fall taps have a ratio of 2:1. The t_{eq} is set to its optimum value of 45ps. Average optical DC power is fixed at 1.5mW and ER at 4dB, for all four measurements.

At 20Gb/s and without equalization the eye is nearly closed (Fig. 8). With equalization the output optical eye improves to 65% horizontal opening, ER of 2.1dB and optical modulation amplitude (OMA) of 0.9dBm. The ratio of the rise and fall taps is again 2:1. Both differential and single-ended operations of the output stage are verified. The VCSEL output stage in single-ended mode draws 5.5mA from a 2.5V power supply. The rest of the equalization

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	JSSC 08 [4]	MTT 10 [3]	ISSCC 13 [5]	ISSCC 14 [6]
Technology	**CMOS SOI 32nm**	CMOS 90nm	CMOS 90nm	CMOS 65nm	SiGe 0.13µm
Supply Voltage (V)	**1.0/2.5**	1.0/2.8	1.0/-	1.2/3.6	2.5/3.3
Data Rate (Gb/s)	**20**	16	10	25	40
Power (pJ/b)	**0.77**	3.0	5.0	3.96	7.80
OMA (dBm)	**0.9**	1.4	2.5	0.8	2.3

circuitry consumes 1.6mW from a 1V supply. This translates to an efficiency of 0.77pJ/b. The maximum data-rate of 20Gb/s is limited by the bandwidth of the VCSEL. Performance summary and comparison are presented in Table I.

VII. CONCLUSION

A novel VCSEL modeling and an efficient equalization technique that takes into account the inherent nonlinearity in the VCSEL's frequency response are presented. The time domain optical responses based on the dynamic VCSEL model verify that the nonlinearity becomes more severe at low VCSEL currents. The rising and falling edges are equalized separately and the equalization delay was selected based on the bias current of the VCSEL. The equalization technique is used to achieve energy efficiency of 0.77pJ/b at 20Gb/s.

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