A Fully Intraocular High-Density Self-Calibrating Epiretinal Prosthesis

Manuel Monge, *Student Member, IEEE*, Mayank Raj, *Student Member, IEEE*, Meisam Honarvar Nazari, *Member, IEEE*, Han-Chieh Chang, *Member, IEEE*, Yu Zhao, *Student Member, IEEE*, James D. Weiland, *Senior Member, IEEE*, Mark S. Humayun, *Fellow, IEEE*, Yu-Chong Tai, *Fellow, IEEE*, and Azita Emami, *Member, IEEE*

***Abstract*—This paper presents a fully intraocular self-calibrating epiretinal prosthesis with 512 independent channels in 65 nm CMOS. A novel digital calibration technique matches the biphasic currents of each channel independently while the calibration circuitry is shared among every 4 channels. Dual-band telemetry for power and data with on-chip rectifier and clock recovery reduces the number of off-chip components. The rectifier utilizes unidirectional switches to prevent reverse conduction loss in the power transistors and achieves an efficiency $> 80\%$. The data telemetry implements a phase-shift keying (PSK) modulation scheme and supports data rates up to 20 Mb/s. The system occupies an area of $4.5 \times 3.1\ \mathrm{mm}^2$. It features a pixel size of $0.0169\ \mathrm{mm}^2$ and arbitrary waveform generation per channel. *In vitro* measurements performed on a Pt/Ir concentric bipolar electrode in phosphate buffered saline (PBS) are presented. A statistical measurement over 40 channels from 5 different chips shows a current mismatch with $\mu = 1.12\ \mu\mathrm{A}$ and $\sigma = 0.53\ \mu\mathrm{A}$. The chip is integrated with flexible MEMS origami coils and parylene substrate to provide a fully intraocular implant.**

***Index Terms*—Biomedical, calibration, data telemetry, epiretinal prosthesis, implantable biomedical devices, neural interfaces, neural prosthesis, neural stimulator, neurostimulator, power telemetry, retinal prosthesis, self-calibrating.**

I. Introduction

RETINAL degenerative diseases such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD) are leading causes of blindness [1], affecting millions worldwide. RP and AMD damage the photoreceptor cells (rods and cones) resulting in profound vision loss, but leave the inner retinal cells (bipolar, horizontal and ganglion cells) functional [2]–[4]. Retinal prostheses Fig. 1 aim to restore vision in these patients by bypassing the damaged photoreceptors and directly stimulating the remaining healthy neurons. There are three main approaches in retinal prostheses which are based on the location of the electrode array: epiretinal, subretinal and suprachoroidal approaches. In an epiretinal prosthesis the electrode array is placed in front of the retina, in a subretinal prosthesis it is placed between the retina and the retinal pigment epithelium, and in a suprachoroidal prosthesis it is placed between the choroidal and the sclera. Each method presents different requirements in terms of space, medical procedures, and electrode-tissue interface [5], and each has its own advantages and disadvantages. Further discussions on these techniques are well summarized in [1], [5]–[20].

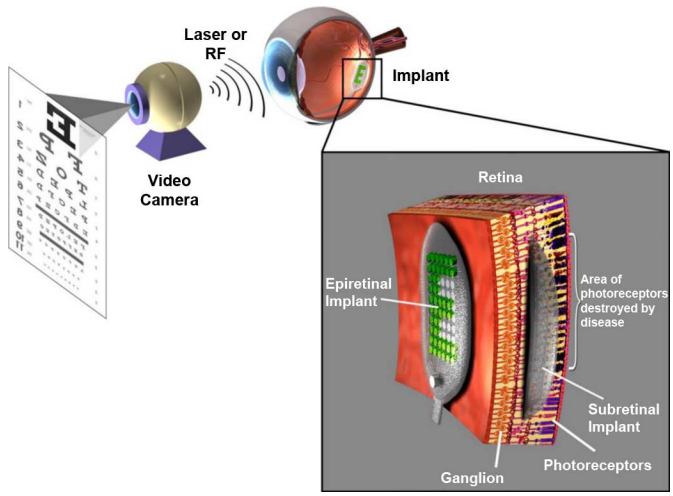

Fig. 1. Retinal Prosthesis (Image courtesy of [15]).

The prosthesis stimulates the retina using electrical stimulation. Fig. 2(a) shows a model of the stimulator array and the electrode-retina interface. This interface presents a high impedance as a result of the small size of the electrode ($100\ \mu\mathrm{m}$ diameter). The stimulator, which can be modeled as a charge-pump, generates a biphasic current waveform to stimulate the retina Fig. 2(b). During the first phase, charge is injected into the tissue, which changes the membrane potential of adjacent cells and makes them fire. In the second phase, this charge is removed from the tissue reducing the residual charge close to zero. This is important because any remaining

Manuscript received October 18, 2013; revised December 10, 2013; accepted December 19, 2013. Date of publication January 20, 2014; date of current version January 28, 2014. This work was supported by NSF Biomimetic Micro-Electronic Systems—Engineering Research Center (BMES-ERC). This paper was recommended by Associate Editor S. Gambini.

M. Monge, M. Raj, M. H. Nazari, H.-C. Chang, Y. Zhao, and A. Emami are with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: mmonge@caltech.edu; makk@caltech.edu; meisam@caltech.edu; jaychang@caltech.edu; yzhao@caltech.edu; azita@caltech.edu).

J. D. Weiland and M. S. Humayun are with the Department of Ophthalmology and Biomedical Engineering, University of Southern California, Los Angeles, CA 90033 USA (e-mail: jweiland@usc.edu; humayun@med.usc.edu).

Y.-C. Tai is with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA 91125 USA, and also with the Department of Bioengineering and Mechanical Engineering, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: yctai@caltech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2014.2298334

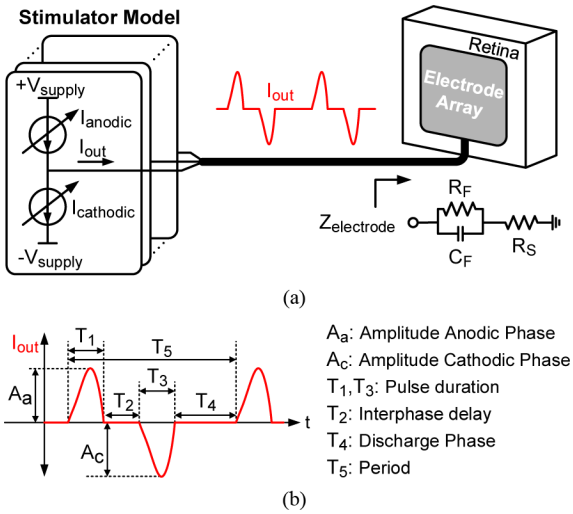

Fig. 2. (a) Model of the stimulator array and electrode-retina interface, where C_F represents the double-layer capacitance, R_F the faradaic charge transfer, and R_S the solution impedance. (b) Stimulation current waveform.

charge beyond tolerable limits can cause electrolysis that may result in tissue damage and electrode corrosion. Therefore, charge-balanced stimulation is essential and requires anodic and cathodic currents to be equal. Another significant characteristic is the stimulation waveform. The shape and duration of each phase, as well as the interphase delay and the period are important stimulation parameters. Several studies have shown that more sophisticated waveforms such as high-frequency pulse trains, asymmetric biphasic pulses, or non-rectangular shapes (Gaussian, linear and exponential), present advantages over biphasic pulses [21]–[24]. A recent publication [25] has proved that flexible stimulation such as step-down current pulse shape can potentially reduce the required voltage compliance by 10%-15%. Thus, having a highly flexible stimulation waveform is desirable and allows further studies in stimulation efficiency, color perception and multi-channel stimulation [5], [24], [26].

Recent work on retinal prostheses has shown significant progress over the past decade. Clinical trials have proven to successfully provide visual restoration with an acuity on the order of 20/1200 to blind patients suffering from retinal degeneration [1]. Simulation studies in normally sighted subjects have predicted that hundreds of channels are needed to restore functional visual perception to a degree that will enable tasks such as reading and face recognition [20]. In recent epiretinal prostheses, the number of electrodes has increased considerably, achieving up to 1024 channels [27] using a 1:4 demux scheme and limiting the functionality of the system to biphasic pulses. However, previous work has used extraocular implants with a trans-sclera trans-choroid cable to connect the electrode array to the retina [11], [12], [17], [28]. Although this method results in a less invasive surgery [12], this cable can cause infection and low intraocular pressure (hypotony) in the long term. To avoid the use of such a cable, a fully intraocular implant is desired. Intraocular coils as well as low power and small size electronics are needed. The former requires the development of high-Q flexible intraocular coils. For the latter, it is essential to reduce off-chip components such as crystal oscillators and diodes, and to make the chip smaller and low power.

Initial designs targeted current levels up to 1 mA to ensure stimulation of retinal cells. For such designs, an output compliance of $>$ 10 V was required [24], [28] due to the high impedance of the electrode-retina interface Fig. 2(a). Therefore, high-voltage (HV) technologies were used at the expense of area and power consumption [5], [24], [28]–[30]. Human clinical trials have recently shown that implanted electrodes present a stimulus threshold as low as 20 μA for a 260 μm diameter electrode implanted in the macular region [20], [31]. In addition, advances in implant technology promise close placement of the electrode array and retinal tissue, which can further decrease the required current. This opens a window for highly scaled technologies to reduce area and power, and to support hundreds of flexible channels for fully intraocular implants.

In this work, a fully intraocular high-density self-calibrating epiretinal prosthesis implemented in 65 nm CMOS is presented. It provides charge-balanced stimulation with highly flexible waveforms. It features dual-band telemetry for power and data, on-chip rectifier and clock recovery, a digital calibration technique to match biphasic stimulation currents, and 512 independent channels capable of arbitrary waveform generation. This paper is organized as follows. Section II describes the system architecture. Section III reviews the calibration methods for neural stimulators and presents the proposed calibration scheme. Detailed circuit-level implementation of the proposed self-calibrating stimulator is presented in Section IV. *In vitro* experimental results using a Pt/Ir bipolar electrode in PBS and comparison with the state of the art are presented in Section V. Finally, Section VI summarizes the work presenting the conclusions.

II. System Architecture

The system architecture of the fully intraocular implant is shown in Fig. 3. It consists of two intraocular coils, the 65 nm IC, off-chip capacitors, electrode array, and the biocompatible flexible parylene substrate. Power and data are wirelessly transmitted to the implant using dual-band telemetry via a pair of inductively coupled coils. The power telemetry operates at 10 MHz and produces 4 different supplies: ± 2 Vdd for stimulation and $\pm$Vdd for the rest of the system. The data telemetry recovers the clock from the power signal and produces 160 MHz and 20 MHz clocks. These signals are used by the phase-shift keying (PSK) receiver to demodulate the 20 Mb/s data. The stimulator array presents 512 independent channels which are grouped into 8 blocks of 16 4-channel stimulators. The global logic receives and demultiplexes the data to each block, running at 20 MHz.

A. 3-Coil Power Transmission

Fig. 4 shows the 3-coil power transmission scheme [32]. The transmitter coil (L1) has an outer diameter (OD) of 42 mm and is placed on external eye-glasses. The buffer coil (L2) is smaller (20 mm OD) and is placed inside contact lenses. The intraocular receiver coil (L3) is a flexible MEMS origami foil coil. It is placed in the anterior chamber of the eye after the crystalline

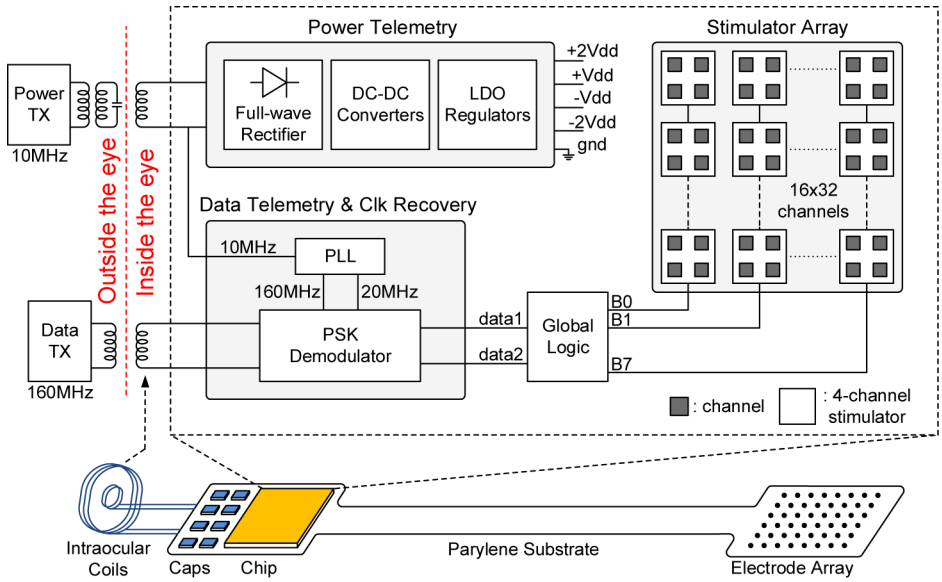

Fig. 3. Fully intraocular epiretinal prosthesis system architecture (modified from [26]).

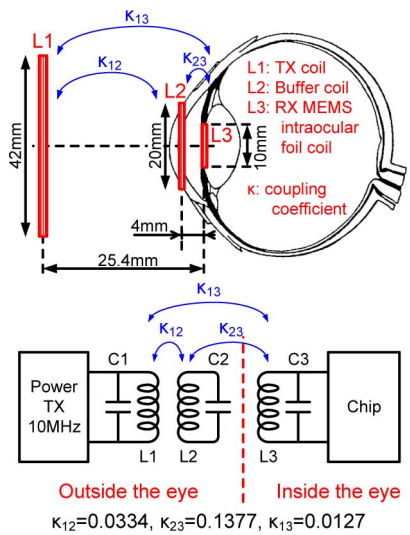

Fig. 4. Three-coil inductive power transmission (modified from [26]).

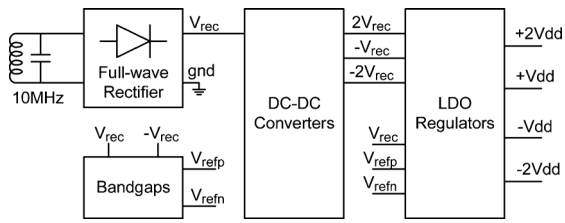

Fig. 5. Schematic of the power telemetry. DC-DC conversion sequence: $\mathrm{V_{rec}} \rightarrow 2\mathrm{V_{rec}}, \mathrm{V_{rec}} \rightarrow -\mathrm{V_{rec}}, -\mathrm{V_{rec}} \rightarrow -2\mathrm{V_{rec}}$ (modified from [26]).

lens is removed. This imposes hard constrains on its size ($<$ 10 mm OD) and weight ($<$ 46 mg in saline). The intraocular coil presents a Q of 24 at 10 MHz in air, 10 mg of mass in saline, and a size of 10 mm OD and 1 mm thickness. The distance between L1 and L3 and the small size and weight of the latter reduces the coupling coefficient κ_{13} drastically. The insertion of the buffer coil enhances coupling coefficients κ_{12} and κ_{23} due to its high Q and close proximity to the eye. This scheme achieves an efficiency of 36% with 1 inch separation in saline, showing a 5x improvement over the 2-coil scheme [32]. It is comparable to the 40% efficiency of the extraocular 2-coil scheme with 18 mm separation presented in [33]. Capacitors C1, C2 and C3 resonate coils L1, L2 and L3, respectevely. Further information about the 3-coil power transmission scheme can be found in [32].

B. Power Telemetry

The power telemetry Fig. 5 operates at 10 MHz. It consists of a full-wave rectifier, a positive and a negative bandgap reference, three DC-DC converters and four low-dropout (LDO) regulators. To reduce the number of off-chip components, an on-chip rectifier was implemented to replace the external diodes used in previous designs [5], [11], [17], [28]. It rectifies the incoming power signal to output $\mathrm{V_{rec}}$ which is then used by the DC-DC converters to generate $-\mathrm{V_{rec}}$ and $\pm 2\mathrm{V_{rec}}$. These signals are used by the LDO regulators to produce the supplies $\pm\mathrm{Vdd}$ and $\pm 2\,\mathrm{Vdd}$. Reference voltages for the LDO regulators are generated by the bandgaps. The rectifier, DC-DC converters and LDO regulators are optimized for efficiency achieving $> 80\%$, $> 90\%$ and $> 85\%$, respectively, for a total combine efficiency of 65%.

The schematic of the proposed full-wave rectifier is shown in Fig. 6(a). In order to increase the efficiency of this stage, two unidirectional switches are used to prevent reverse conduction loss in the power transistors. A comparison between a pass transistor switch and the proposed unidirectional switch Fig. 6(b) shows the advantages of the latter over a traditional implementation. In a pass transistor switch, when $\mathrm{V_{inn}} < \mathrm{V_{rec}} < \mathrm{V_{inp}}$, the transistor M0 is in forward conduction and power is transferred from the input to the output. However, when $\mathrm{V_{inp}}$ decreases lower than $\mathrm{V_{rec}}$ while $\mathrm{V_{inn}}$ is still low ($\mathrm{V_{inn}} < \mathrm{V_{inp}} <$

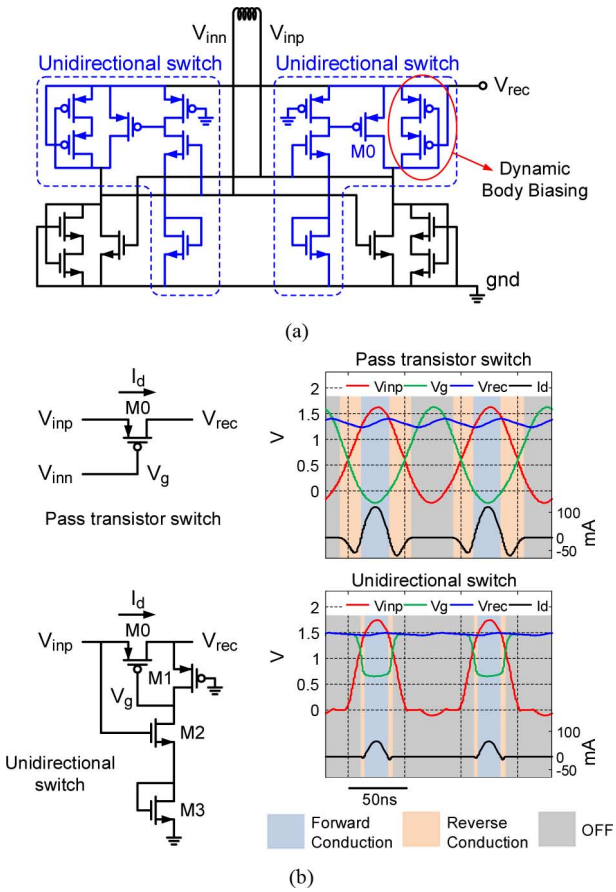

Fig. 6. (a) Transistor-level schematic of the proposed full-wave rectifier (modified from [26]). (b) Comparison between the pass transistor switch and the unidirectional switch showing the reduction in reverse conduction loss.

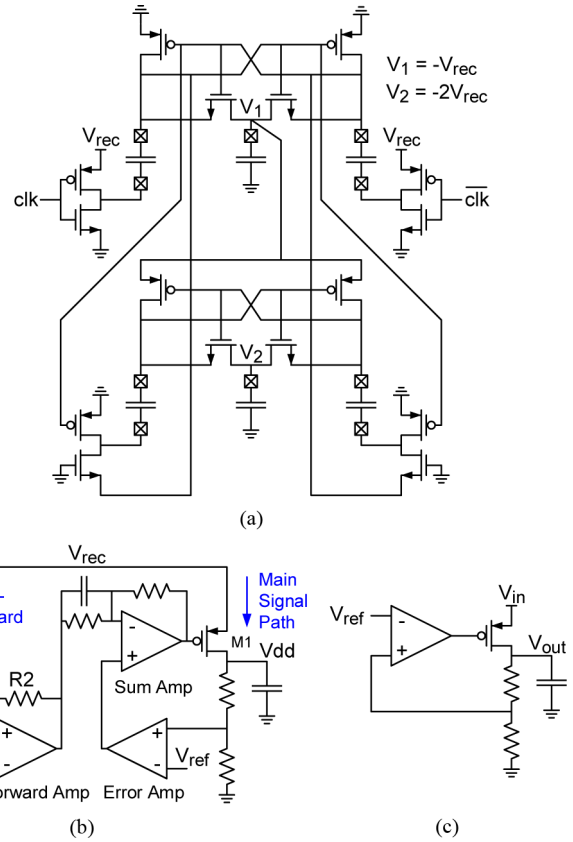

Fig. 7. Schematics of the (a) charge-pump DC-DC converter that generates $-\mathrm{V_{rec}}$ and $-2\mathrm{V_{rec}}$, (b) feed-forward ripple cancellation LDO regulator that generates Vdd (modified from [26]), and (c) LDO regulator that generates -Vdd and $\pm 2\ \mathrm{Vdd}$.

$\mathrm{V_{rec}}$), reverse conduction occurs. This is not desired and reduces the efficiency of the stage considerably. In the proposed switch, reverse conduction is minimized by the addition of transistors M1-M3. When $\mathrm{V_{inp}} < 2\mathrm{V_{th}}$, transistors M2 and M3 are off and leave transistor M1 on. This transistor shorts the gate of the power transistor M0 to $\mathrm{V_{rec}}$ and turns it off. When $\mathrm{V_{inp}} > 2\mathrm{V_{th}}$, transistors M2 and M3 turn on, turning M0 on by reducing its gate voltage. Therefore, forward conduction occurs when $\mathrm{V_{inp}} > \mathrm{V_{rec}} > 2\mathrm{V_{th}}$ while reverse conduction is limited to $\mathrm{V_{rec}} > \mathrm{V_{inp}} > 2\mathrm{V_{th}}$. Simulation results are also shown in Fig. 6(b). A color scheme shows the three regions of operation of the switch: forward conduction, reverse conduction and cut-off. It can be seen that the reverse conduction region is minimized when the unidirectional switches are used. This technique improves the efficiency of the stage to more than 80% while delivering $\approx 25\ \mathrm{mW}$.

The DC-DC converters are implemented using charge-pump circuits. A single stage charge-pump circuit is used to generate $+2\mathrm{V_{rec}}$ while two stages of charge-pump are cascaded to generate $\mathrm{V_{rec}}$ and $-2\mathrm{V_{rec}}$ from the output of the rectifier. This last charge-pump circuit is shown in Fig. 7(a).

The regulator that generates Vdd employs a feed-forward ripple cancellation scheme and is shown in Fig. 7(b). This technique filters out the input ripples by replicating the same ripples at the gate of transistor M1 through the feed-forward path. Resistors R1 and R2 set the feed-forward gain to cancel the noise from the main signal path. In addition, due to the inherent high bandwidth of the feed-forward configuration, significant PSRR is achieved at high frequencies [34]. To further enhance the PSRR bandwidth, a zero is introduced in the summing amplifier to cancel the dominant pole of the system. Three additional regulators, as shown in Fig. 7(c), are employed to generate -Vdd and $\pm 2\ \mathrm{Vdd}$ for the stimulation circuitry.

C. Data Telemetry

The schematic of the data telemetry is shown in Fig. 8(a). It implements a pseudo-differential PSK demodulator with gain control and a PLL for clock recovery. The multiplication factor in the PLL allows for the use of the 10 MHz power signal as a reference to generate I/Q 160 MHz clocks for down-conversion and a 20 MHz clock for the data slicers. This alleviates the need for an external reference which, in previous designs, was provided by an external crystal oscillator [27], [28]. The LNA Fig. 8(b) is a single-ended cascode amplifier with gain control. The gain control is obtained by a 3-bit programmable bias scheme. These bits modify the transconductance of M1 by changing its bias voltage and drain current, providing a minimum gain of 10. The LNA presents a narrow-band $50\ \Omega$ input impedance at 160 MHz set by the capacitor C, the transistor M1, the bias network, and the external coil. The buffer Fig. 8(c) is

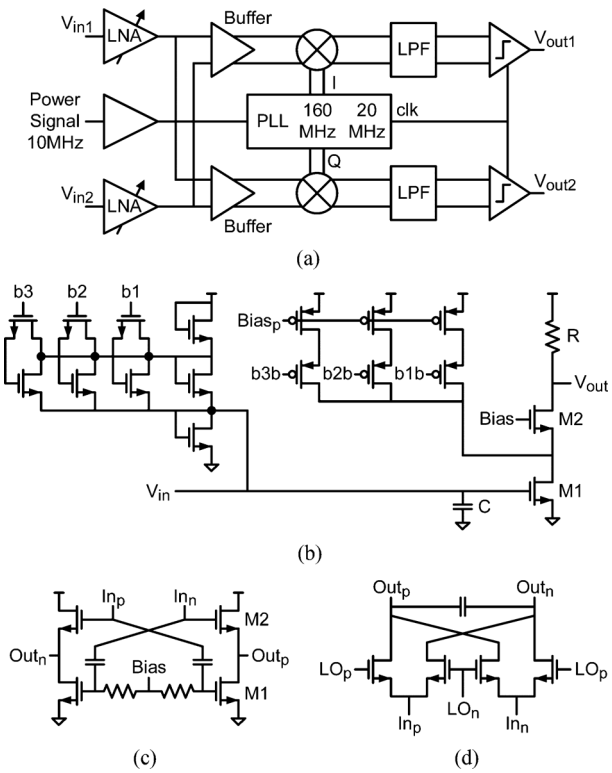

Fig. 8. Schematic of the (a) data telemetry and clock recovery [26], (b) LNA with gain control, (c) differential buffer, and (d) passive-mixer.

a hybrid differential common-source/common-drain amplifier which improves the voltage-gain to $A_v \approx -(g_{m1}+g_{m2})/g_{m2}$. The output of each buffer is then mixed by a passive-mixer with the I/Q 160 MHz clocks, respectively. Passive-mixers Fig. 8(d) were chosen to reduce power consumption. The size of the mixer switches is optimized to minimize the voltage drop and non-linearity effects. The low-pass filter is added at the output of the mixer and is implemented by a passive RC-filter. The low-power sense amplifier is a standard Strong-Arm latch followed by a SR latch.

Given the following input signals:

$$V_{\text{in1}}(t) = A\sin(\omega t + \phi_1) \tag{1}$$
$$V_{\text{in2}}(t) = A\cos(\omega t + \phi_2) \tag{2}$$

where A is the amplitude of the received signal and $\phi_1, \phi_2 \in \{0°, 180°\}$, the datapath produces 2 data streams

$$V_{\text{out1}}(t) = \frac{AA_T}{2}\cos(\phi_1) = \pm\frac{AA_T}{2} \tag{3}$$
$$V_{\text{out2}}(t) = -\frac{AA_T}{2}\cos(\phi_2) = \mp\frac{AA_T}{2} \tag{4}$$

where $A_T = A_{\text{LNA}} \cdot A_{\text{Buffer}}$. Each data stream supports data rates up to 20 Mb/s, for a combine data rate of 40 Mb/s, although only 20 Mb/s is required for single-chip operation. The datapath and PLL consume 2.3 mA and 350 μA, respectively.

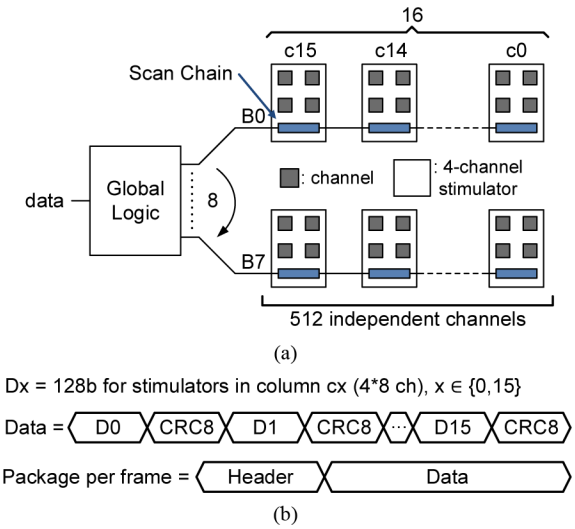

Fig. 9. (a) Schematic of the global logic and stimulator array showing scan chain connections. (b) Communication protocol for data transmission.

D. Stimulator Array

The stimulator array, shown in Fig. 9(a), is composed of 512 independent channels grouped into 8 blocks. Each block consists of 16 4-channel stimulators, which are explained in detail in Section III and Section IV. The input of each stimulator is serialized and connected to all stimulators in the same block. This makes a 256-bit scan chain per block (4-bit per channel). The 8 scan chains are connected to the outputs of the global logic. The global logic receives the demodulated data, processes it and demultiplexes it into 8 bit streams running at 20 MHz. It implements the communication protocol shown in Fig. 9(b). In case of communication error, the whole package is discarded, the scan chains are reset, and all the stimulators receive a zero input.

In this work a high resolution current-based stimulation scheme has been utilized. The voltage-based stimulation technique reported in [35] promises high energy-efficiency, but it is more suitable for relatively long stimulation pulses (more than 8 ms). A global reference current, generated by the bandgap, is distributed to each stimulator using a tree structure. Cascode current mirrors with transistors biased in strong inversion are used to minimize current variations. Simulation results showed that the reference current at each 4-channel stimulator has a $\sigma = 21.7$ nA while distributing 1.3 μA.

E. Multi-Chip Configuration

An additional feature of the system is its capability for 2-chip configuration in a Master/Slave fashion. In this case, both coils (power and data) are connected to the master chip which generates the supplies and demodulates the data. In particular, it produces 2 data streams V_{out1} and V_{out2}Fig. 8(a) according to (3) and (4). One of them is used in the master chip while the other is sent to the slave chip. The power and data telemetry circuits in the slave chip are shut down, since it receives the supplies and data stream from the master chip. Thus, both chips can be integrated in parylene to support 1024 independent channels. As the number of required electrodes for retinal prosthesis continues to increase, this technique will allow the use of multiple chips to

configure a network to scale up the number of channels of the design with only minor modifications.

III. Calibration Methods for Neural Stimulators

Matching the current or charge of biphasic stimulation is an important design consideration in neural implants. Previous studies in cochlear implants have shown that a residual DC current of more than 100 nA is highly correlated with neural tissue damage [36] and that this value has been suggested as a safety limit [37]–[39]. However, a safety limit for retinal prosthesis has not been established yet and it depends on electrode material, electrode size and shape, as well as charge density [40], [41].

A large DC blocking capacitor in series with the electrode can reduce the residual DC current to minimal levels (< 1 nA)[30], but hundreds of capacitors in the nF range are not realizable for retinal prostheses [42]. Simple passive charge-balancing techniques rely on shorting the stimulation electrode to the counter electrode. The effectiveness of this technique depends on the initial charge imbalance, the time constant associated with the electrode-tissue interface, and the available time for the discharge phase [30]. The charge error after stimulation $\mathrm{Q_{error}}$ is caused by the mismatch between anodic and cathodic currents, and the difference between the duration of each phase. For example, a 5 μA mismatch between stimulation currents in a 2 ms 100 Hz biphasic pulse with 1 ms duration at each phase (i.e., pulse duration difference is negligible) generates a $\mathrm{Q_{error}} = 5\ \mu\mathrm{A} \times 1\ \mathrm{ms} = 5\ \mathrm{nC}$. Assuming there is no interface delay, the discharge phase is $\tau_{\mathrm{discharge}} = 10\ \mathrm{ms} - 2\ \mathrm{ms} = 8\ \mathrm{ms}$. For a stimulation period T and a time constant $\tau = (\mathrm{R_{SW}} + \mathrm{R_S}) \times \mathrm{C_F} = 3\ \mathrm{ms}$, where $\mathrm{R_{SW}}$ is the shorting switch resistance, $\mathrm{R_S}$ is the tissue resistance and $\mathrm{C_F}$ represents the double-layer capacitance of the interface, the net DC current error is defined as

$$I_{\mathrm{DCerror}} = \frac{Q_{\mathrm{remained}}}{T} = \frac{Q_{\mathrm{error}} \cdot e^{-\tau_{\mathrm{discharge}}/\tau}}{T} \qquad (5)$$

which is equal to 34.74 nA. Although this value is less than 100 nA, for reasons of patient safety, it is desirable to achieve a more precise charge balance with a DC current error close to the level produced by DC blocking capacitors [30]. Therefore, it is important to reduce the initial charge imbalance by matching anodic and cathodic currents with high precision [5], [24].

A. Previous Work

Several methods to achieve charge-balanced stimulation have been reported in the literature. An analog negative feedback technique to sample and hold a correction current to improve current matching has been used in [29]. A similar technique, dynamic current matching, is used in [30]. Here, a single DAC generates the cathodic current which is sampled by a pmos transistor to produce the anodic current. These schemes require the use of large capacitors to store the sampled voltage for the duration of both phases. This increases the area of the stimulator considerably, making them not suitable for a multi-channel implant. They also need to run for every stimulation which increases the power consumption. Furthermore, they rely on constant output current that limits them to biphasic pulses.

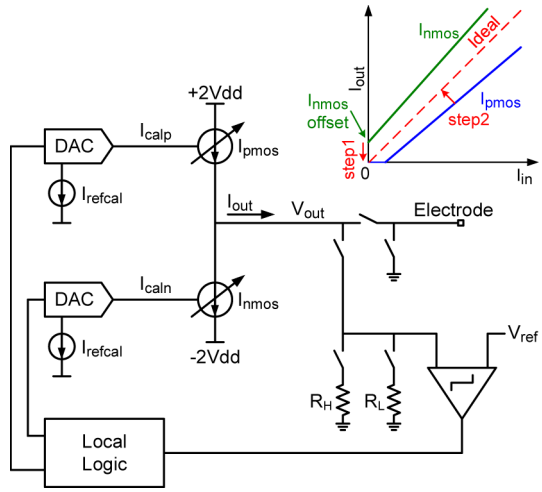

Fig. 10. Model of the proposed calibration scheme and illustration of the non-ideal initial characteristics of $\mathrm{I_{nmos}}$ and $\mathrm{I_{pmos}}$ due to process variation.

Active charge balancers [5], [24] monitor any residual charge in the tissue after every stimulation and keep this charge within a safety window of $\approx \pm 100$ mV. Two different approaches have been presented: Active charge balancers based on pulse insertion and based on offset regulation. The former cancels the remaining charge instantaneously via short current pulses [5] while the latter cancels the remaining charge in the long-term by adjusting the offset of the stimulation currents [24], [43]. The precision of charge balance in this technique is a function of the capacitance of the electrode-tissue interface [30]. In addition, this compensation depends on the output waveform and changes for different wave shapes.

In this work, we propose a digital calibration technique to match anodic ($\mathrm{I_{pmos}}$) and cathodic ($\mathrm{I_{nmos}}$) currents, and to reduce area and power consumption. The calibration needs to run only once when the implant is turned on (e.g., daily).

B. Two-Step Digital Calibration Scheme

A model of the stimulator connected to the calibration circuitry is shown in Fig. 10. Two switched resistors are used to sense the output current $\mathrm{I_{out}}$ during calibration. The high resistor R_H increases the conversion gain when $\mathrm{I_{out}}$ is low, while the low resistor R_L ensures voltage compliance when $\mathrm{I_{out}}$ is high. This measured voltage ($\mathrm{V_{out}}$) is then compared to $\mathrm{V_{ref}}$ to produce a digital output that is sent to the local logic. Based on this result, the local logic adjusts two current DACs to calibrate the stimulation currents. As illustrated in the same figure, anodic and cathodic currents differ from an ideal behavior due to process variation. To compensate for this difference, a two-step digital calibration scheme is proposed. During the first step, the offset of $\mathrm{I_{nmos}}$, which is the current value at zero input, is cancelled. In the second step, $\mathrm{I_{pmos}}$ is matched to $\mathrm{I_{nmos}}$ by reducing their difference ($\mathrm{I_{diff}}$).

1) Step 1: To measure the offset of $\mathrm{I_{nmos}}$, R_H is connected to the output, a zero input is set, and the $\mathrm{I_{nmos}}$ current source is turned on. As a result, the offset of $\mathrm{I_{nmos}}$ flows to R_H. The voltage across this resistor ($\mathrm{V_{out}}$) is then compared to $\mathrm{V_{ref}}$.

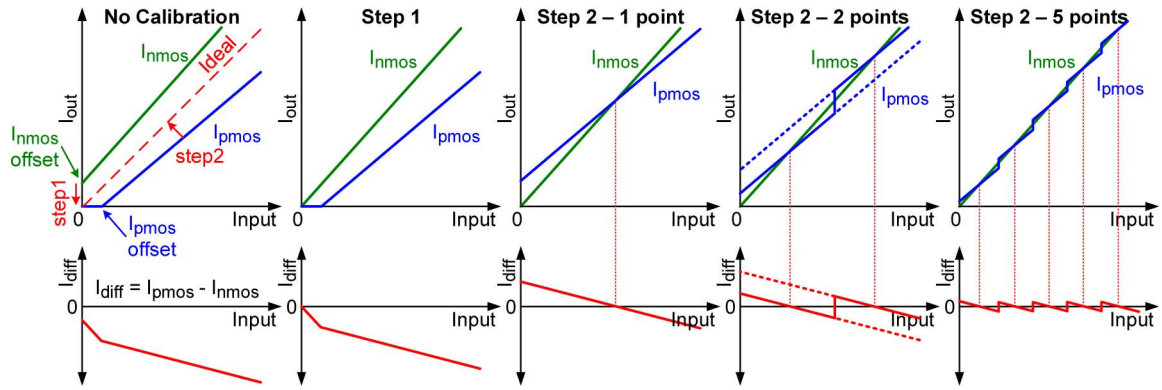

Fig. 11. Conceptual model of the two-step multi-point calibration scheme [26].

Based on this, the calibration current I_{caln} is changed to adjust I_{nmos} until the comparator switches. Finally, the value of the calibration DAC is stored in a local register. For this step, V_{ref} is set to $-\Delta V$ to account for the fact that the offset of I_{nmos} flows from R_H to the current source making V_{out} always negative. In order to switch the comparator, V_{out} is compared to a small negative voltage so that, when the offset gets reduced, the comparator switches.

2) Step 2: To measure I_{diff}, R_L is connected to the output and both currents are turned on so that I_{diff} flows to R_L. Using the same method as the previous case with V_{ref} set to 0 V (since I_{diff} can flow in both directions), the calibration current I_{calp} is adjusted to reduce I_{diff}. Then, the calibration value is also stored in a local register.

3) Multi-Point Calibration: Since the slope of the two currents can vary, reducing I_{diff} at one point does not guarantee to match them over the entire range. To overcome this issue, the output current range is split into regions and a distinct calibration is performed for each region. By increasing the number of calibration points, the overall difference of the currents I_{diff} gets reduced over the entire range. In this design, for the target mismatch of $< 5\%$ that correspond to $2.5\ \mu$A, a 5-point calibration scheme was chosen.

Fig. 11 illustrates the conceptual model of the calibration scheme. Simulation results from a Montecarlo simulation are shown in Fig. 12. The calibration scheme was able to adjust the currents in all cases and achieve significant improvement in matching. The current mismatch after calibration has a mean (μ) of $0.78\ \mu$A and standard deviation (σ) of $0.52\ \mu$A. Details of the implementation and analysis of the effects of process variation in the calibration scheme are explained in Section IV-B.

IV. Self-Calibrating 4-Channel Stimulator

The circuit level implementation of the proposed stimulator is shown in Fig. 13. It consists of 4 independent current drivers, which share calibration circuitry and local logic. Each current driver presents a 5 V output stage and produces an arbitrary output waveform with 4 bits of resolution at $109.2\ \mu$s time-steps. A 4-bit input signal determines the input current I_{in}. This current is mirrored to the output stage to produce either the anodic current I_{pmos} or the cathodic current I_{nmos}, depending on the stimulation phase. The local logic controls the stimulation and the calibration. It has a serial interface that enables the use

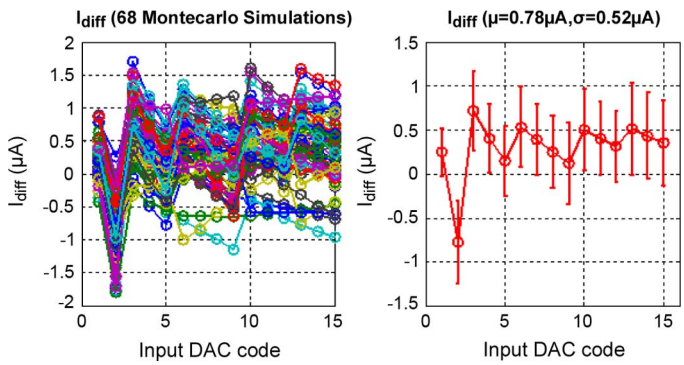

Fig. 12. Montecarlo simulation of the two-step calibration scheme showing a current mismatch with $\mu = 0.78\ \mu$A and $\sigma = 0.52\ \mu$A.

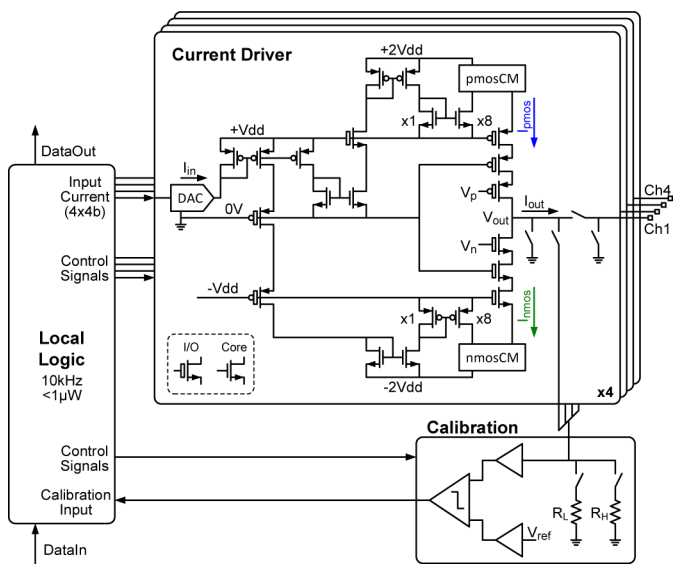

Fig. 13. Detailed schematic of the self-calibrating 4-channel stimulator (modified from [26]).

of simple cascade connections to build the array. It is important to mention that while the calibration circuitry is shared among every 4 channels, each channel is calibrated independently.

A. Current Driver

The schematic of the current driver is shown in Fig. 13. To enable robust operation with high output voltage, low-headroom

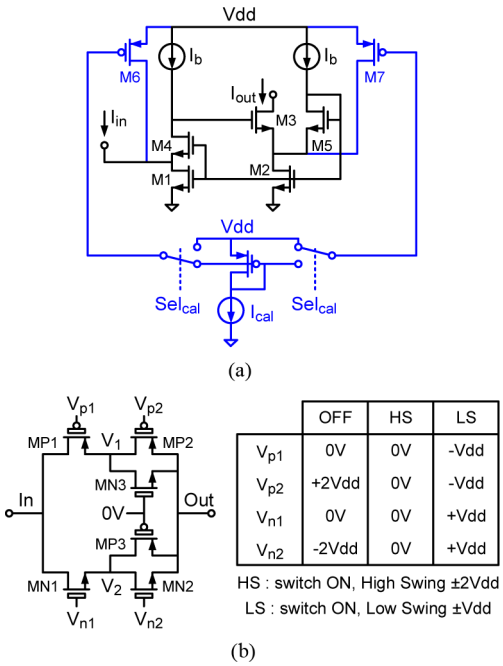

Fig. 14. Schematics of (a) current mirror (modified from [26]) and (b) high-voltage switch.

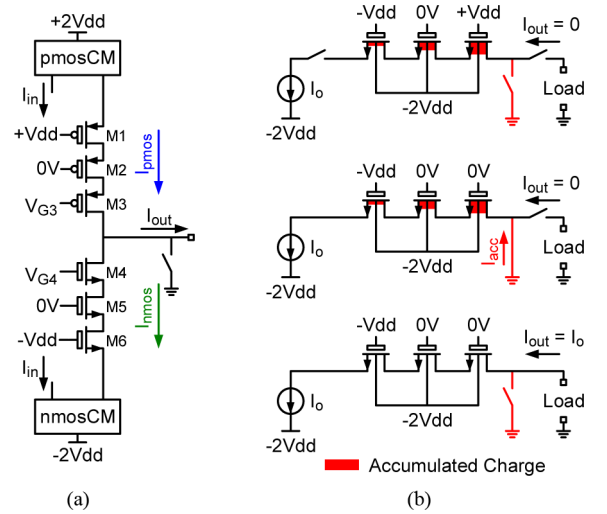

Fig. 15. (a) Schematic of the output stage of the current driver. V_{G3} and V_{G4} are dynamically biased to avoid stressing the transistors. (b) Model of the protection transistors M4-M6 showing how accumulated charge is removed prior to stimulation.

current mirrors and protection transistors have been used. Low-voltage (LV) transistors are used extensively, and high voltage transistors are used only for protection. A 5 V output stage is designed using 1.2 V core and 2.5 V I/O transistors, and is limited by the nwell-substrate junction breakdown voltage (6 V in this process).

Low-headroom current mirrors are used at the output stage to increase the voltage compliance. The current mirror is a variation of [44] and presents a high output resistance with low headroom Fig. 14(a). Two current sources bias transistors M4 and M5 and reduce the drain voltage of M1 and M2 for low-headroom operation. M3 increases the loop gain, which increases the output resistance. The circuit is optimized for low headroom at the expense of higher mismatch. However, this mismatch is compensated by the calibration scheme. Transistors M6 and M7 are added to either increase or decrease I_{out} according to the calibration by mirroring the calibration current I_{cal}.

In order to connect the electrode or the calibration circuit to the current driver, the switches have to tolerate voltages in the range of $V_{out} \in [-2Vdd + V_h, +2Vdd - V_h]$, where V_h is the headroom of the current mirror. A traditional complimentary switch implemented with I/O transitors cannot be used because it will present > 2.5 V between its terminals. To overcome this, a HV switch that limits the voltage between transistor terminals to < 2.5 V has been designed Fig. 14(b). V_{p1} and V_{n1} bias transistors MP1 and MN1 to withstand the input voltage swing, while V_{p2} and V_{n2} open or close the switch. Transistors MN3 and MP3 are used to reduce the voltage at middle nodes (V_1 and V_2) when leakage current flows through the switch. The HV switch has two modes of operation when it is turned on, depending on the required input voltage swing. For a low swing of $\pm$ Vdd (i.e., calibration phase, discharge phase), V_{p1} and V_{p2} are set to -Vdd while V_{n1} and V_{n2} are set to +Vdd. For a higher swing (i.e., stimulation phase), V_{p1}, V_{p2}, V_{n1} and V_{n2} are set to 0 V to withstand the voltage swing. It is important to mention that in this last mode $V_{in} \neq V_{out}$ for $|V_{out}| < |V_{th}|$; nevertheless, $I_{out} = I_{in}$ for all cases.

Fig. 15(a) shows the output stage of the current driver. It is implemented using a stack of 6 I/O transistors. Since the current mirrors are implemented with core transistors, the voltage across them has to be $\leq$ Vdd. To achieve that, the gate voltage of transistors M1 and M6 are set to +Vdd and -Vdd, respectively. To avoid stressing the transistors, the gate voltage of M3 and M4 are dynamically biased according to the stimulation phase, while V_{G2} and V_{G5} are set to 0 V. During anodic phase (I_{pmos} is on and $V_{out} > 0$ V), V_{G3} is set to 0 V turning M3 on. During cathodic phase (I_{pmos} is off and $V_{out} < 0$ V), V_{G3} is set to -Vdd to distribute the almost 5 V (4 Vdd) across transistors M1, M2 and M3 keeping the voltage across the current mirror $\leq$ Vdd. A similar analysis can be done for the I_{nmos} current, setting the values for V_{G4} to be +Vdd and 0 V during anodic and cathodic phase, respectively.

Between stimulation phases (interphase delay and discharge phase), the current driver is disconnected from the electrode and both stimulation currents (I_{pmos} and I_{nmos}) are turned off. In this state, protection transistors in the output stage of the current driver (M1-M6) accumulate charge due to the body effect. Since these transistors share the same substrate (p-well for nmos and n-well for pmos), each transistor accumulates different amount of charge proportional to its V_{GB}. This is shown in Fig. 15(b) for transistors M4-M6, where V_{GB4}, V_{GB5} and V_{GB6} are 3 Vdd, 2 Vdd and Vdd, respectively. The red bar in the figure represents the accumulated charge. In order to guarantee charge-balanced stimulation based on calibrated stimulation currents, this charge is removed via a switch prior to stimulation.

B. Calibration

Fig. 16 shows the schematic of the calibration circuitry connected to the local logic and a simple model of the current

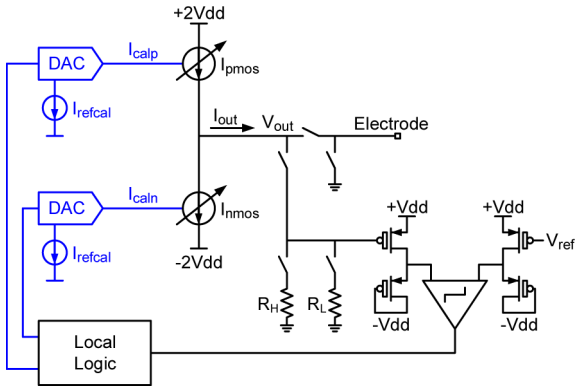

Fig. 16. Schematic of the calibration circuitry.

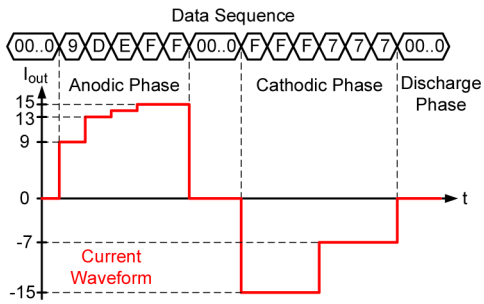

Fig. 17. Arbitrary waveform generation.

driver. R_H and R_L sense the output current $\mathrm{I}_{\mathrm{out}}$. A self-biased pmos common-source amplifier with pmos load, implemented with I/O transistors, is used as a pre-amplifier to provide gain with good linearity and to bias and protect the comparator. A strong-arm sense amplifier is used as the calibration comparator and is implemented using core transistors. In this design, $\mathrm{R}_H = 75\ \mathrm{k}\Omega$, $\mathrm{R}_L = 15\ \mathrm{k}\Omega$, $\mathrm{V}_{\mathrm{ref}} = -35\ \mathrm{mV}$ (step 1) or 0 V (step 2), and the calibration DACs have 5-bit resolution with $\mathrm{I}_{\mathrm{refcal}}$ set to 1 μA.

The resolution of the calibration is set by the minimum detectable voltage $\mathrm{V}_{\mathrm{LSB}}$, which is defined as:

$$V_{\mathrm{LSB}} = I_{\mathrm{refcal}} \cdot R_{H/L} \tag{6}$$

where $\mathrm{I}_{\mathrm{refcal}}$ is the reference current of the calibration DACs and $R_{H/L}$ is R_H or R_L, depending on the calibration step. To maximize current matching, $\mathrm{V}_{\mathrm{LSB}}$ is designed according to the following expression:

$$V_{\mathrm{LSBmin}} > |V_{\mathrm{ref}}|_{\max} + \sum V_{\mathrm{offset}} \tag{7}$$

where

$$\sum V_{\mathrm{offset}} = V_{\mathrm{offset-PreAmps}} + V_{\mathrm{offset-Comparator}}. \tag{8}$$

Thus, the variation of $\mathrm{I}_{\mathrm{refcal}}$ becomes the dominant factor. This variation is minimized by increasing the size of the transistors in the bias network and by distributing a current that bias these

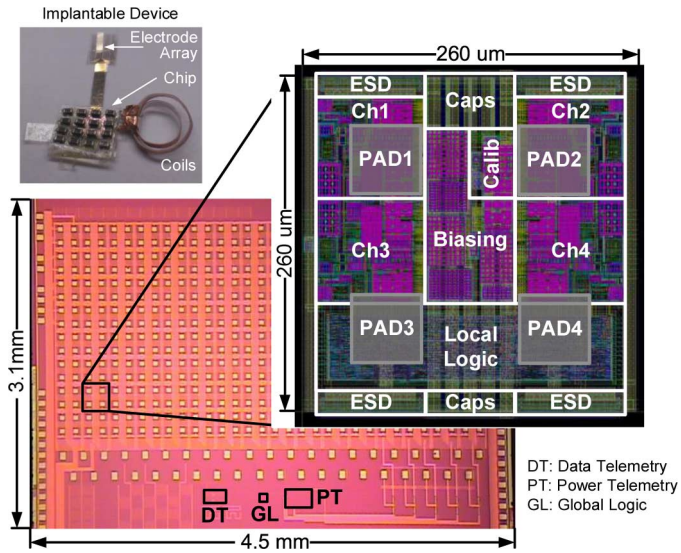

Fig. 18. Die micrograph of the epiretinal prosthesis, layout of the 4-channel stimulator (4 independent channels sharing local logic and calibration circuitry), and picture of the prototype of the implantable system (modified from [26]).

transistors in strong inversion. The drawback is a slightly higher power consumption.

C. Local Logic

The local logic controls the calibration and the stimulation, and stores the calibration values. It runs at a low frequency clock of 10 kHz to save power and consumes < 1 uW, which is mostly due to leakage. It implements six finite state machines (FSM). Four identical FSMs control the current drivers and produce independent channels. A separate FSM controls the calibration of each channel which is performed in a serial fashion. Finally, an arbiter controls the global operation of the local logic.

Fig. 17 shows how the arbitrary output waveform is generated. A data sequence with 4 bits of resolution defines the amplitude of the waveform every 109.2 μs. The first non-zero values correspond to the first phase. Then, a group of zeros sets the interphase delay. The next group of non-zero values defines the second phase. Finally, after both phases, the last group of zeros (discharge phase) ends the biphasic stimulation and shorts the electrode to ground. Any remaining charge imbalance is then removed during this phase.

V. Measurement Results

The prototype was fabricated in a 65 nm LP bulk CMOS process. The die micrograph and stimulator details are presented in Fig. 18. The chip occupies an area of $4.5 \times 3.1\ \mathrm{mm}^2$, including the extra area needed for parylene integration (0.4 mm on the bottom, 0.2 mm on the sides and top). The 4-channel stimulator occupies an area of $260 \times 260\ \mu\mathrm{m}^2$ including pads, ESD structures and bypass capacitors, for a pixel size of $0.0169\ \mathrm{mm}^2$. A picture of the prototype of the implantable device is also shown in the same figure.

The functionality of the system was verified using a 75 μm/300 μm inner/outer diameter Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while the

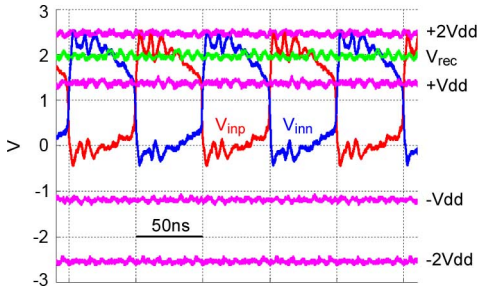

Fig. 19. Measurement of generated supply voltages.

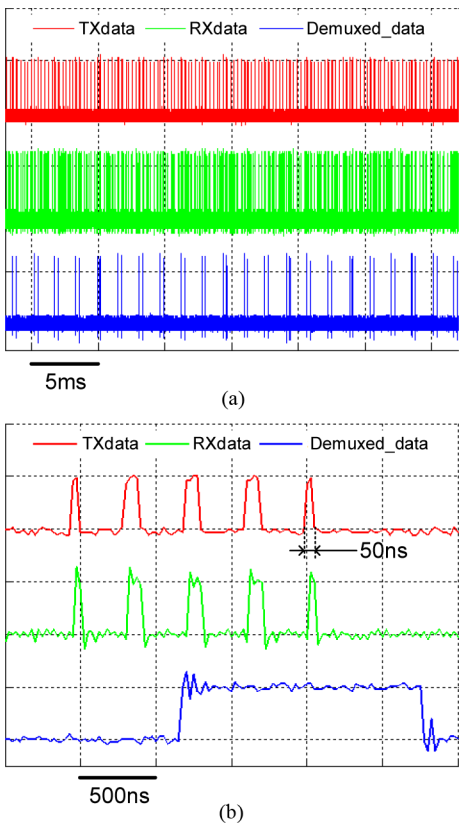

Fig. 20. (a) Measured data telemetry digital signals at 20 Mb/s. (b) Details of the measured signals.

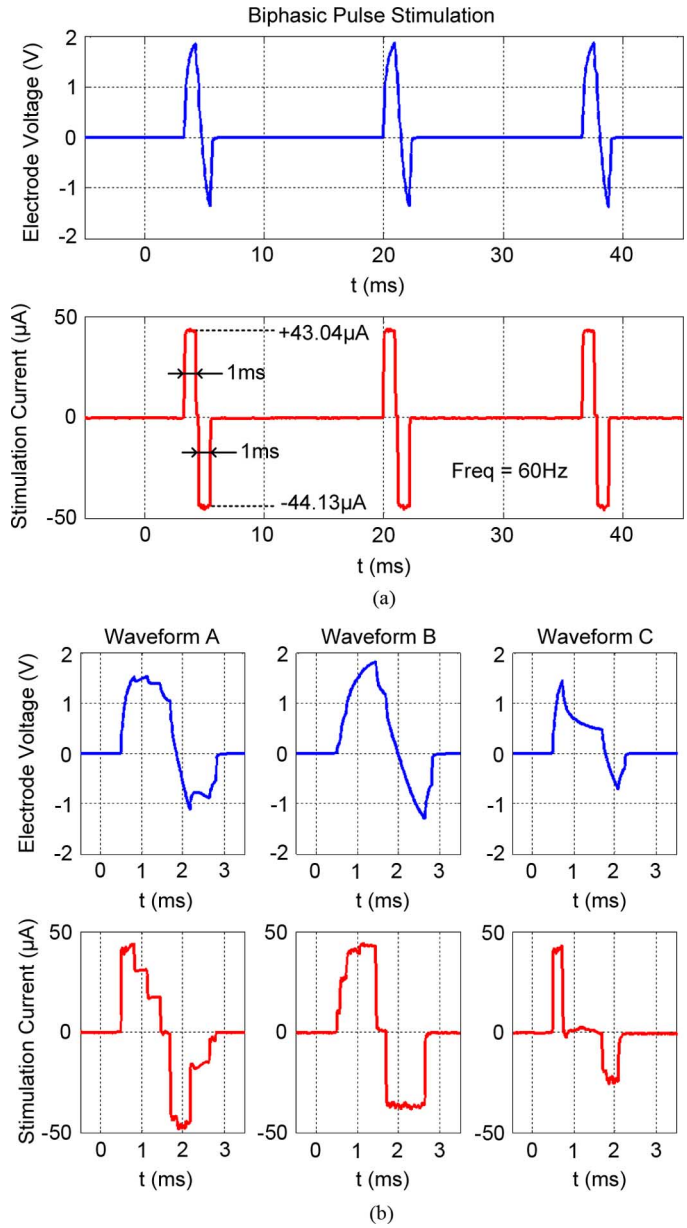

Fig. 21. Measured arbitrary output waveforms using a Pt/Ir flat concentric bipolar electrode in 1X PBS solution as a load while power and data are delivered wirelessly. (a) Biphasic pulse at 60 Hz with a current mismatch of 1.09 μA. (b) 3 different arbitrary waveforms.

implant receives power and data wirelessly. An arbitrary waveform generator was used to generate the PSK modulated data, and a signal generator was used to generate the 10 MHz power signal. The impedance of the electrode-solution interface was measured and fitted to a simple linear model. It shows a solution resistance $\mathrm{R_S}$ of 20 kΩ in series with a faraday capacitance $\mathrm{C_F}$ of 160 nF. This impedance is close to the impedance expected from a 100 μm diameter Pt electrode implanted in the retina, which is 100 nF in series with 30 kΩ[45].

Fig. 19 shows measurements of power telemetry operating at 10 MHz. The rectified voltage ($\mathrm{V_{rec}}$) and the generated supplies ($\pm$Vdd, $\pm$2Vdd) were measured to be $\approx$ 1.97 V, $\approx$ $\pm$1.3 V and $\approx$ $\pm$2.5 V, respectively. Fig. 20 shows measurements of data telemetry. A 20 Mb/s 160 MHz PSK data was sent to the system and was correctly demodulated. Fig. 20(a) shows 35 ms of the measured transmitted signal (TXdata), received signal (RXdata) and demultiplexed signal (Demuxed_data, output of global logic). Fig. 20(b) shows details of these signals.

Measurements of arbitrary output waveforms are shown in Fig. 21. The measured voltages show the integrated version of the current due to the capacitive effect of the electrode-solution interface. First, a biphasic pulse at 60 Hz is generated. Then, three different arbitrary waveforms were sent to the implant using the same setup. A piecewise-constant pulse (Waveform A), a pseudo-exponential pulse followed by a constant pulse (Waveform B), and an asymmetric biphasic pulse (Waveform C) were tested. Measurements show that the chip is capable of arbitrary output waveform generation. The charge error after stimulation $\mathrm{Q_{error}}$ has been estimated by calculating the integral of the stimulation current over the duration of the pulse.

TABLE I
PERFORMANCE COMPARISON — EPIRETINAL PROSTHESIS

	JSSC07 [5]	JSSC10 [28]	ISSCC13 [27]	This Work
Technology	HV 0.35μm	HV 0.18μm	HV 0.18μm	65nm 1.2V/2.5V
Modulation	Photodiode	DPSK @ 22MHz	DPSK	PSK @ 160MHz
Data Rate	968kb/s	2Mb/s	2Mb/s	Up to 20Mbps
Power Carrier	N.A.	2MHz	2MHz	10MHz
On-Chip Supplies (V)	3.3, 11.25, 22.5	$\pm$1.8, $\pm$12	$\pm$1.8, $\pm$12	$\pm$1.3, $\pm$2.5
Number of Channels	232	256	1024	512
I_{out} max (μA)	1000	500	500	50
V_{out} range (V)	>20 (1.25, 21.25)	-10, +10	-10, +10	-2.4, +2.4
Pixel Size (mm^2)	$\approx$0.0718	0.08034	0.026	0.0169
Shared Channels	2*	1	4*	1**
Mismatch	<50μA, charge balancers 5%	<14.5μA <2.9%	N.A.	μ=1.12μA, σ=0.53μA† 2.24%
Load model	10kΩ+100nF	10kΩ+100nF	30kΩ	30kΩ+100nF
Total Area (mm^2)	4.9x4.5	5.3x5.1	5.7x6.6	4.5x3.1††

* no independent channels ** every 4 independent channels share local logic and calibration circuitry

† Statistical measurement (μ: mean, σ: standard deviation)

†† including extra area for placement in parylene (0.4mm on the bottom, 0.2mm on the sides and top)

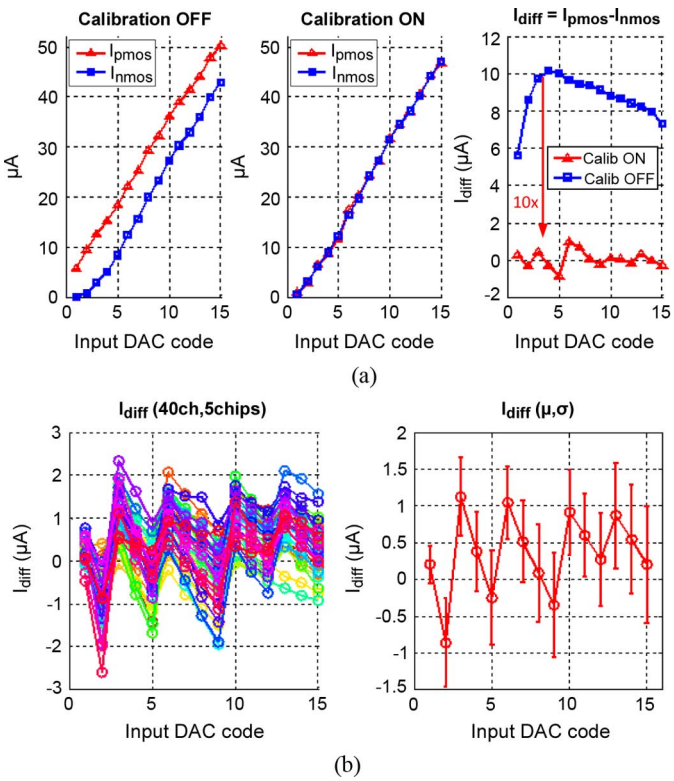

Fig. 22. (a) Measurements of current matching from a single channel showing a 10x improvement when calibration is turned on. (b) Statistical measurement over 40 channels from 5 different chips showing a current mismatch with $\mu = 1.12\ \mu$A and $\sigma = 0.53\ \mu$A[26].

The biphasic pulse, waveform A, B and C have an estimated Q_{error} of 0.7 nC, 1.09 nC, 0.23 nC and 1.2 nC, respectively.

Fig. 22(a) shows the performance of the calibration technique on a single channel. I_{pmos} and I_{nmos} currents were measured for each value of the input DAC with the calibration turned on and off. The figure shows that both currents are monotonic and that the matching of the currents is improved by a factor of 10 when the calibration is turned on (mismatch decreased from 10 μA to 1 μA). A statistical measurement over 40 channels from 5 different chips was performed and is shown in Fig. 22(b). All 40 channels were correctly calibrated and present a current mismatch with $\mu = 1.12\ \mu$A and $\sigma = 0.53\ \mu$A. This measurement shows good alignment with the simulation results shown in Fig. 12. Differences are mainly caused by the variation of I_{refcal} due to the bias network, which was not considered in the simulation.

The power consumption of the system depends on the stimulation waveform and the number of active channels (activity factor). The system is one of the most power efficient designs, consuming 15 mW for a 10% duty cycle, 50 μA biphasic pulse at 50% activity factor. The output voltage range was also measured after replacing the electrode-solution load by a resistive load. The maximum and minimum output voltage, voltage headroom and output impedance were measured to be ± 2.4 V, 0.1 V and greater than 1 MΩ, respectively.

Table I summarizes the performance of the proposed epiretinal prosthesis and compares it with the state of the art. The self-calibrating 4-channel stimulator is also compared with the state of the art neural stimulators in Table II. The system achieves a reduction of 35% in pixel size. It is important to note that none of the previous work in the literature has reported statistical measurements for current matching.

VI. CONCLUSION

A high-density 512-channel self-calibrating epiretinal prosthesis chip fabricated in 65 nm LP CMOS has been presented. The complete system includes high-data rate data telemetry, low-power clock recovery, and high-efficiency power telemetry. The addition of the on-chip rectifier and clock recovery reduce off-chip components such as diodes and crystal oscillator. A two-step digital calibration technique that matches stimulation currents is introduced. This technique is shown to be robust against process variation and achieves a current mismatch with a mean of 1.12 μA and standard deviation of 0.53 μA. The local logic and calibration circuitry are shared among every 4

TABLE II
PERFORMANCE COMPARISON — STIMULATOR IC

	ISCAS07 [29]	TBCAS07 [30]	JSSC10 [28]	EMBC11†† [46]	JSSC12 [24]	ISSCC13 [27]	TBCAS13†† [47]	This Work
Technology	HV 0.5μm	HV 0.7μm	HV 0.18μm	65nm	HV 0.35μm	HV 0.18μm	HV 0.35μm	65nm 1.2V/2.5V
Supplies (V)	$\pm$3, $\pm$8	-9, +6	$\pm$1.8, $\pm$12	+1 ,+3.3	3.3,10,17,20	$\pm$1.8, $\pm$12	3, 12, 15	$\pm$1.3, $\pm$2.5
V_{out} range (V)	-7.45, +7.45	-8, 5	-10, +10	-1.5, +1.5	0.3, 19.7	-10, +10	0.8, 14.2	-2.4, +2.4
Pixel Size (mm^2)	0.51	1.44	0.08034	0.04	0.05875	0.026	0.1	0.0169
Shared Channels	1	1	1	1	4*	4*	1	1**
I_{out} max	3.2mA	1mA	500μA	N.A.	1mA	500μA	1mA	50μA
Mismatch	1.8μA 0.05625%	4μA 0.4%	<14.5μA <2.9%	N.A.	charge balancers	N.A.	<1μA <0.3%	μ=1.12μA, σ=0.53μA† 2.24%
Load model	N.A.	3.9kΩ+10nF	10kΩ+100nF	N.A.	10kΩ+100nF	30kΩ	10kΩ+100nF	30kΩ+100nF

* no independent channels ** every 4 independent channels share local logic and calibration circuitry

† Statistical measurement (μ: mean, σ: standard deviation) †† two electrodes per stimulation point

channels to reduce power and area. The chip features a pixel size of $0.0169\ \mathrm{mm}^2$ resulting in a total area of $4.5 \times 3.1\ \mathrm{mm}^2$. It also supports a master/slave configuration which extends the design to 1024 channels. The system is integrated with MEMS origami coils and off-chip capacitors using a biocompatible flexible parylene substrate. All components fit inside the eye providing a fully intraocular implant. *In vitro* measurement results conducted on a Pt/Ir concentric bipolar electrode in PBS solution validated the functionality of the system.

ACKNOWLEDGMENT

The authors acknowledge the contributions of M. Loh and J. Yoo for insightful technical discussions, A. Wang for assistance with the experimental work, and TSMC for chip fabrication.

REFERENCES

[1] K. Mathieson, J. Loudin, G. Goetz, P. Huie, L. Wang, T. Kamins, L. Galambos, R. Smith, J. Harris, A. Sher, and D. Palanker, "Photovoltaic retinal prosthesis with high pixel density," *Nature Photon.*, vol. 6, no. 6, pp. 391–397, May 2012.

[2] S. Y. Kim, S. Sadda, J. Pearlman, M. Humayun, E. d. Juan, B. M. Melia, and W. R. Green, "Morphometric analysis of the macula in eyes with disciform agerelated macular degeneration," *Retina*, vol. 22, pp. 471–477, 2002.

[3] F. Mazzoni, E. Novelli, and E. Strettoi, "Retinal ganglion cells survive and maintain normal dendritic morphology in a mouse model of inherited photoreceptor degeneration," *J. Neurosci.*, vol. 28, pp. 14282–92, 2008.

[4] J. L. Stone, W. Barlow, M. Humayun, E. de Juan, and A. Milam, "Morphometric analysis of macular photoreceptors and ganglion cells in retinas with retinitis pigmentosa," *Arch. of Ophthalmol.*, vol. 110, pp. 1634–39, 1992.

[5] M. Ortmanns, A. Rocke, M. Gehrke, and H. J. Tiedtke, "A 232-Channel epiretinal stimulator ASIC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2946–2959, Dec. 2007.

[6] J. Ohta, T. Noda, K. Sasagawa, T. Tokuda, Y. Terasawa, H. Kanda, and T. Fujikado, "A CMOS microchip-based retinal prosthetic device for large numbers of stimulation in wide area," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2013, pp. 642–645.

[7] T. Tokuda, Y. Takeuchi, T. Noda, K. Sasagawa, K. Nishida, Y. Kitaguchi, T. Fujikado, Y. Tano, and J. Ohta, "Light-controlled retinal stimulation on rabbit using CMOS-based flexible multi-chip stimulator," in *Proc. 31st Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Sep. 2009.

[8] Y. T. Wong, S. C. Chen, Y. A. Kerdraon, P. J. Allen, M. F. McCombe, J. W. Morley, N. H. Lovell, and G. J. Suaning, "Efficacy of supra-choroidal, bipolar, electrical stimulation in a vision prosthesis," in *Proc. 30th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Aug. 2008.

[9] L. H. Jung, N. Shany, T. Lehmann, P. Preston, N. H. Lovell, and G. J. Suaning, "Towards a chip scale neurostimulator: System architecture of a current-driven 98 channel neurostimulator via a two-wire interface," in *Proc. 33rd Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, 2011.

[10] A. Rothermal, V. Wieczorek, L. Liu, A. Stett, M. Gerhardt, A. Harscher, and S. Kibbel, "A 1600-pixel subretinal chip with DC-free terminals and ± 2 V supply optimized for long lifetime and high stimulation efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 144–602.

[11] L. Theogarajan, "A low-power fully implantable 15-Channel retinal stimulator chip," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2322–2337, Oct. 2008.

[12] S. K. Kelly, D. B. Shire, J. Chen, P. Doyle, M. D. Gingerich, S. F. Cogan, W. A. Drohan, S. Behan, L. Theogarajan, J. L. Wyatt, and J. F. Rizzo, "A hermetic wireless subretinal neurostimulator for vision prostheses," *IEEE Trans. Biomed. Eng.*, vol. 58, no. 11, pp. 3197–3205, Nov. 2011.

[13] H. G. Graf, C. Harendt, T. Engelhardt, C. Scherjon, K. Warkentin, H. Richter, and J. N. Burghartz, "High dynamic range CMOS imager technologies for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 281–289, Jan. 2009.

[14] J. D. Loudin, S. F. Cogan, K. Mathieson, A. Sher, and D. V. Palanker, "Photodiode circuits for retinal prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 5, pp. 468–480, Oct. 2011.

[15] J. Weiland, W. Liu, and M. Humayun, "Retinal prosthesis," *Annu. Rev. Biomed. Eng.*, vol. 7, pp. 361–401, 2005.

[16] E. Zrenner, "Will retinal implants restore vision?," *Science*, vol. 295, no. 5557, pp. 1022–1025, 2002.

[17] W. Liu and M. Humayun, "Retinal prosthesis," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 15–19, 2004, vol. 1, pp. 218–219.

[18] J. L. Wyatt, "Engineering development of a subretinal prosthesis," in *Proc. 2nd DOE Int. Symp. Artificial Sight*, 2005, p. 55.

[19] J. Rizzo, "Retinal prosthesis: An encouraging first decade with major challenges ahead," *Ophthalmol.*, vol. 108, no. 1, pp. 13–14, 2001.

[20] J. Weiland and M. Humayun, "Visual prosthesis," *Proc. IEEE*, vol. 96, no. 7, pp. 1076–1084, 2008.

[21] W. M. Grill and J. T. Mortimer, "Stimulus waveforms for selective neural stimulation," *IEEE Eng. Med. Biol. Mag.*, vol. 14, no. 4, pp. 375–385, 1995.

[22] A. Wongsarnpigoon, J. P. Woock, and W. M. Grill, "Efficiency analysis of waveform shape for electrical excitation of nerve fibers," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 18, pp. 319–328, Jun. 2010.

[23] M. Sahin and Y. Tie, "Non-rectangular waveforms for neural stimulation with practical electrodes," *J. Neural Eng.*, vol. 4, pp. 227–233, May 2007.

[24] E. Noorsal, K. Sooksood, X. Hongcheng, R. Hornig, J. Becker, and M. Ortmanns, "A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 244–256, 2012.
[25] M. E. Halpern and J. Fallon, "Current waveforms for neural stimulation-charge delivery with reduced maximum electrode voltage," *IEEE Trans. Biomed. Eng.*, vol. 57, no. 9, pp. 2304–2312, Sep. 2010.
[26] M. Monge, M. Raj, M. H. Nazari, H.-C. Chang, Y. Zhao, J. Weiland, M. Humayun, Y.-C. Tai, and A. Emami-Neyestanak, "A fully intraocular $0.0169\ \mathrm{mm}^2/\mathrm{pixel}$ 512-channel self-calibrating epiretinal prosthesis in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 17-21, 2013, pp. 296–297.
[27] K. Chen, Y.-K. Lo, and W. Liu, "A $37.6\ \mathrm{mm}^2$ 1024-channel high-compliance-voltage SoC for epiretinal prostheses," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 17-21, 2013, pp. 294–295.
[28] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, "An integrated 256-Channel epiretinal prosthesis," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1946–1956, 2010.
[29] E. K. F. Lee and A. Lam, "A matching technique for biphasic stimulation pulse," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2007, pp. 817–820.
[30] J.-j. Sit and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 nA DC error for 1-mA full-scale stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 172–183, 2007.
[31] A. Horsager, S. H. Greenwald, J. Weiland, M. Humayun, R. J. Greenberg, M. J. McMahon, G. M. Boynton, and I. Fine, "Predicting visual sensitivity in retinal prosthesis patients," *Invest. Ophthalmol. Vis Sci*, vol. 50, pp. 1483–1491, 2009.
[32] Y. Zhao, M. Nandra, C. C. Yu, and Y. C. TaI, "High performance 3-Coil wireless power transfer system for the 512-electrode epiretinal prosthesis," in *Proc. Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, 2012, pp. 6583–6586.
[33] K. Chen, Y. K. Lo, Z. Yang, J. Weiland, M. Humayun, and W. Liu, "A system verification platform for high-density epiretinal prostheses," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 326–337, Jun. 2013.
[34] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.
[35] S. K. Kelly and J. L. Wyatt, "A power-efficient neural tissue stimulator with energy recovery," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 20–29, Feb. 2011.
[36] R. K. Shepherd, N. Linahan, J. Xu, G. M. Clark, and S. Araki, "Chronic electrical stimulation of the auditory nerve using noncharge-balanced stimuli," *Acta Otolaryngologica*, vol. 119, pp. 674–684, 1999.
[37] R. Shepherd, B. Franz, and G. Clark, "The biocompatibility and safety of cochlear prostheses," *Cochlear Prostheses*, pp. 69–98, 1990.
[38] J. Xu, R. K. Sheperd, R. E. Millard, and G. M. Clark, "Chronic electrical stimulation of the auditory nerve at high stimulus rates: a physiological and histopathological study," *Hear. Res.*, vol. 105, no. 1, pp. 1–29, 1997.
[39] C. Q. Huang, P. M. Carter, and R. K. Shepherd, "Stimulus induced ph changes in cochlear implants: An in vitro and in vivo study," *Ann. Biomed. Eng.*, vol. 29, no. 9, pp. 791–802, 2001.
[40] S. F. Cogan, "Neural stimulation and recording electrodes," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 275–309, 2008.
[41] S. Negi, R. Bhandari, L. Rieth, R. V. Wagenen, and F. Solzbacher, "Neural electrode degradation from continuous electrical stimulation: Comparison of sputtered and activated iridium oxide," *J. Neurosci. Methods*, vol. 186, no. 1, pp. 8–17, 2010.
[42] G. J. Suaning and N. H. Lovell, "CMOS neurostimulation asic with 100 channels, scalable output, and bidirectional radio-frequency telemetry," *IEEE Trans. Biomed. Eng.*, vol. 48, no. 2, pp. 248–260, Feb. 2001.
[43] K. Sooksood, T. Stieglitz, and M. Ortmanns, "An active approach for charge balancing in functional electrical stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 162–170, Jun. 2011.
[44] L. F. Tanguay, M. Sawan, and Y. Savaria, "A very-high output impedance current mirror for very-low voltage biomedical analog circuits," in *Proc. IEEE Asia Pacific Conf. Circuits and Systems*, 2008, pp. 642–645.
[45] S. Shah, A. Hines, D. Zhou, R. J. Greenberg, M. Humayun, and J. Weiland, "Electrical properties of retinal-electrode interface," *J. Neural Eng.*, vol. 4, pp. S24–9, Mar. 2007.
[46] N. Tran, E. Skafidas, J. Yang, S. Bai, M. Fu, D. Ng, M. Halpern, and I. Mareels, "A prototype 64-electrode stimulator in 65 nm CMOS process towards a high density epi-retinal prosthesis," in *Proc. Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, 2011, pp. 6729–6732.
[47] H. Chun, Y. Yang, and T. Lehmann, "Safety ensuring retinal prosthesis with precise charge balance and low power consumption," *IEEE Trans. Biomed. Circuits Syst.*, 2013, IEEE Early Access article.

Manuel Monge (S'09) received the B.S. degree (with honors) in electrical engineering from the Pontifical Catholic University of Peru (PUCP), Lima, Peru, and the M.S. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2010, respectively.

Currently, he is working toward the Ph.D. degree in electrical engineering at Caltech. His research interests are analog and mixed-signal circuits and systems, with focus on process variation correction, biomedical circuits and neural interfaces. He spent the summer of 2013 at Samsung Display America Laboratory (SDAL) working on on-chip channel monitoring circuits for high-speed links.

Mr. Monge received the 2008 PUCP Best Student Award and 2008 Fulbright Peru Opportunity Grant Scholarship. He is recipient of the 2009 Caltech Atwood Fellowship and third place winner of the 2013 Broadcom Foundation University Research Competition.

Mayank Raj (S'08) received the B.Tech. degree from the Indian Institute of Technology (IIT), Kanpur, India, and the M.S. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2009, respectively.

Currently, he is working toward the Ph.D. degree at Caltech. The focus of his current research is high-performance mixed-signal integrated circuits for high-speed and low-power optical and electrical interconnects. He spent the summer of 2012 at Xilinx Inc. working on on-chip noise monitoring circuits.

Mr. Raj was the recipient of the 2008 Caltech Atwood Fellowship and 2012 Patent Achievement Award from Xilinx Inc.

Meisam Honarvar Nazari (S'08–M'13) received the B.Sc. degree from the University of Tehran, Tehran, Iran, in 2005, the M.A.Sc. degree from the University of Toronto, Toronto, ON, Canada, in 2008, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2009 and 2013, respectively.

Currently, he is a Postdoctoral Sscholar at Caltech. The focus of his current research is biomedical microsystems for health care monitoring. He spent the summer of 2011 at Rambus Inc., where he worked on new equalization techniques for high data rate communication links.

Mr. Nazari received the University of Toronto Fellowship for Fall 2006 and an Atwood fellowship for Fall 2008. He was the corecipient of 2008 Brian L. Barge Award for excellence in microsystems integration, 2010 AMD/CICC Student Scholarship Award, the 2012 Solid-State Circuits Society Award, and the 2012 Circuits and Systems Society predoctoral scholarship. He was also an NVIDIA 2012 graduate fellowship finalist.

Han-Chieh Chang (S'04–M'13) was born in Taipei, Taiwan, in 1982. He received the B.S. degree in mechanical engineering from National Taiwan University (NTU), Taiwan, and the Ph.D. degree in electrical engineering from the California Institute of Technology (Caltech), in 2004 and 2013, respectively.

He has authored papers in more than 15 technical publications and has five pending U.S. patent applications. While pursuing the Ph.D. degree, he was funded by the National Science Foundation (NSF), working on the Biomimetic MicroElectronic Systems (BMES) project

collaborated with the University of Southern California, Los Angeles, CA, USA, with emphasis on retinal prosthesis. Since September 2013, he has held a postdoctoral position with the Department of Electrical Engineering at Caltech.. His research interests focus on developing innovative MEMS devices for medical application using semiconductor processing.

Yu Zhao (S'07) received the B.S. degree (with honors) in microelectronics from Peking University, Beijing, China, and the M.S. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2008 and 2009 respectively.

While pursuing the Ph.D. degree at Caltech, she has been working on the wireless power transfer scheme for intraocular retinal prostheses, wireless intraocular pressure sensor, catheter-based impedance sensor for intravascular plaque, and wireless ECG recording implant for zebra fish. Her research interests focus on developing micro implants for biomedical applications, which involves front-end sensor fabrication, flexible circuitry design, and assemble wireless power and data telemetries.

James D. Weiland (SM'08) received the B.S. degree in 1988, M.S. degrees in biomedical engineering in 1993 and electrical engineering in 1995, and the Ph.D. degree in 1997, all from the University of Michigan, Ann Arbor, MI, USA.

After receiving the B.S. degree, he worked four years in industry with Pratt & Whitney Aircraft Engines. He joined the Wilmer Ophthalmological Institute at The Johns Hopkins University, Baltimore, MD, USA, in 1997 as a Postdoctoral Fellow and, in 1999, was appointed an Assistant Professor of Ophthalmology at Johns Hopkins. He was appointed Assistant Professor at the Doheny Eye Institute at the University of Southern California (USC), Los Angeles, CA, USA, in 2001. Currently, he is a Professor of Ophthalmology and Biomedical Engineering at USC. He is Deputy Director of the Biomimetic Microelectronic Systems Engineering Research Center. His research interests include retinal prostheses, neural prostheses, electrode technology, visual evoked responses, implantable electrical systems, and wearable visual aids for the blind.

Dr. Weiland is a Senior Member of the IEEE Engineering in Medicine and Biology Society, the Biomedical Engineering Society, Sigma Xi, and the Association for Research in Vision and Ophthalmology.

Mark S. Humayun (M'97–SM'10–F'12) received the B.S. degree from Georgetown University, Washington, DC, USA, the M.D. degree from Duke University, Durham, NC, USA, and the Ph.D. degree from the University of North Carolina, Chapel Hill, NC, USA, in 1984, 1989, and 1994, respectively.

He is the Director of the University of Southern California (USC), Los Angeles, CA, USA, Eye Institute and the USC Sensory Science Institute, Interim Chair of the Department of Ophthalmology of USC, current holder of the Cornelius J. Pings Chair in Biomedical Sciences, and Professor of Ophthalmology and Biomedical Engineering at USC. His research focuses at the intersection of engineering and medicine on the development of biomimetic bioelectronics for medical applications with a special focus on ophthalmological and neurological diseases. He is the founding director of the NSF ERC Biomimetic Microelectronic Systems Engineering Research Center. He has more than 150 peer-reviewed publications, authored more than 20 book chapters and is listed as an inventor on more than 100 patents/patents applications. His work has led to the formation of multiple start-up companies. He is recognized internationally as the inventor of an artificial bioelectronic retina to restore sight to the blind. The artificial retina called Argus II was recently approved by FDA as the first bioelectronics retinal implant to restore sight to certain blind patients.

Dr. Humayun is a member of the National Academies of Engineering and the National Academies Institute of Medicine. He was named inventor of the year by *R&D Magazine* in 2005. *U.S. News and World Report* listed him in the top one percent of ophthalmologists in 2011.

Yu-Chong Tai (M'97–SM'03–F'06) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, Berkeley, CA, USA, in 1982, 1986, and 1989, respectively.

He is currently a Professor of electrical engineering, mechanical engineering, and bioengineering at the California Institute of Technology (Caltech), Pasadena, CA, USA. He developed the first electrically spun polysilicon micromotor at the University of California, Berkeley. At Caltech, his main research interest is MEMS for biomedical applications, including lab-on-a-chip and microimplants. He has authored more than 300 technical articles in the field of MEMS.

Dr. Tai was the recipient of the IBM Fellowship, Ross Tucker Award, Best Thesis Award (at Berkeley), Presidential Young Investigator Award, Packard Award, and ALA Achievement Award.

Azita Emami (S'97–M'04) received the B.S. degree (with honors) from Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1996, 1999 and 2004, respectively.

Currently, she is a Professor of Electrical Engineering at the California Institute of Technology (Caltech), Pasadena, CA, USA. From July 2006 to August 2007 she was with Columbia University, New York, NY, USA, as an Assistant Professor in the Department of Electrical Engineering. She also worked as a Research Staff Member at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, from 2004 to 2006. Her current research areas are high-performance mixed-signal integrated circuits and VLSI systems, with focus on high-speed and low-power optical and electrical interconnects, clocking circuits, biomedical implants and sensors, drug delivery systems, and compressed sensing.