A Low-Noise Fully Differential Recycling Folded Cascode Neural Amplifier

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***Abstract*—This paper describes the design of an amplifier to be used as part of a neural recording system. The architecture of this amplifier was based on a fully differential folded cascode (FDFC) amplifier and adapted to a recycling architecture [1] which reuses currents in order to achieve better performance. Furthermore, as we are designing a neural amplifier, a low input-referred noise is required due to the small amplitude of neural signals, as they could be as small as 1 μV. The recycling architecture was optimized for low-noise, and simulated in *AMS* 0.35 μm CMOS process. An input-referred noise of 1.16 μV_{rms} was achieved while consuming 66.03 μW from a 3.3 V supply, which corresponds to NEF=2.58. The open-loop gain of the amplifier is 111.25 dB and the closed-loop gain is 42.10 dB with a bandwidth of 6.02 kHz.**

***Index Terms*—Neural Amplifier, Recycling, Low Noise, Fully Differential, Folded Cascode.**

I. Introduction

The miniaturization capability of transistors has introduced microelectronics into the field of medicine and neuroscience. Nowadays, it is very common to talk about implantable integrated circuits for electrocardiograms (ECG) or neural signal recording. The latter is known as a neural acquisition system and the data provided by this kind of circuits have led to a better understanding of brain disorders and the nervous system. Recently, many institutions have shown their interest in brain research and have acknowledged its importance. The three major projects in neural signals are: The Human Brain Project [2], DARPA SyNAPSE Program [3] and The BRIAN Initiative [4]. The accurate measure of neural signals is critical for these projects and the development of more efficient acquisition systems is necessary.

According to their electric characteristics, the electric potentials of neural signals are classified in two types: Action Potentials (AP) and Low Field Potentials (LFP). APs, also known as "spikes", are transient signals and their duration ranges from 0.3 to 1 ms [5]. This type of potential is associated with the activation of individual neurons. The magnitude of APs could range from 10 μV to 1 mV, and appear in the high frequency region from 300 Hz to 6 kHz [6]. On the other hand, LFPs have slower oscillations than APs with an amplitude that could range from 1 mV to 10 mV [1]. They represent an average of the neural activity in the proximity of an electrode. This type of signals belongs to a lower frequency band, from less than 1 Hz to 200 Hz [6]. Both, APs and LFPs are significantly affected by noise because of their small amplitude.

This paper reports the design of a fully differential folded cascode amplifier based on the recycling architecture described in [1]. Nonetheless, this referenced work was not proposed as a neural amplifier, thus it does not consider noise as a critical parameter. The architecture of the circuit is shown in Figure 1, and we will refer to it as the fully differential recycling folded cascode (FDRFC). The parameter K in Figure 1 refers to the current gain in the recycling path and, in reference [1], it is equal to 3 in order to use the same current budget of a conventional folded cascode amplifier for a fair comparison. However, an analysis for the optimal value of K is realized in this paper to enhance the performance. Section II describes this analysis, Section III shows simulation results of amplifiers with K=1.5, 2, 3 and 5, and compares them with the state-of-the-art. Finally, Section IV presents the conclusions.

II. Design of the Neural Amplifier

A. Specifications of the amplifier

The recycling architecture in which are based our amplifiers has exhibited an improvement in gain and bandwidth. This is due to the current mirrors M3a-M3b and M4a-M4b in which currents are reused or recycled in contrast to the conventional architecture of a FDFC [1]. However, the result of the analysis of the input-referred noise is not conclusive and our design focus on minimize it. For an adequate performance of the acquisition system, the requirement is that the input-referred noise should be less than extracellular and electrodes background noise, approximately 5 – 10 μV_{rms} [7].

Another requirement for the design is to achieve a gain sufficiently high to amplify the neural signal. They are in the range of micro and millivolts so we consider that a close-loop gain of 40 dB is enough for the pre-amplification stage of the acquisition system. The output voltage of the amplifier is acceptable as input voltage for a posterior stage which might involve an ADC or another amplification stage. The bandwidth should be at least 6 kHz as explained in [6].

B. Circuit analysis

The analysis of this circuit is similar to the conventional folded cascode but considering the recycling path to enhance performance. From Figure 1 we can see that transconductance of transistors M1a, M1b, M2a and M2b should be equal to

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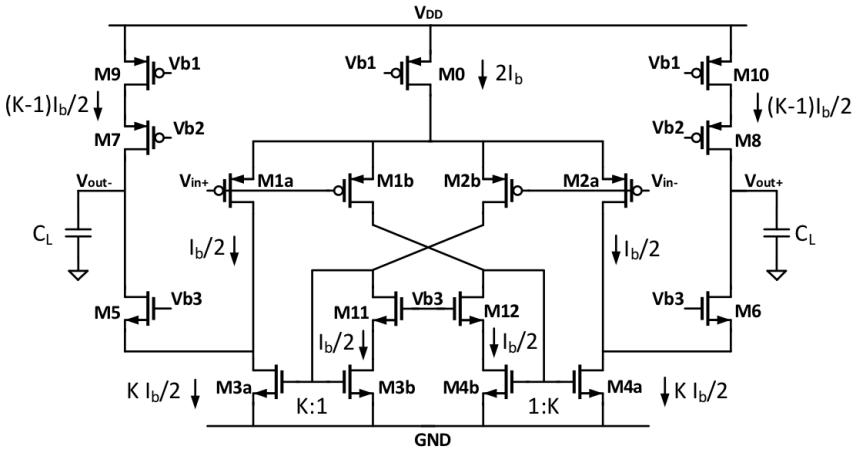

Fig. 1. The Fully Differential Recycling Folded Cascode (FDRFC) amplifier

have the same strength on both, the main and recycling path. Because this is a fully differential amplifier, the circuit has symmetry for its left and right side, thus they have same model parameters (e.g. gm, r_o, etc.).

The following metrics of the amplifier are obtained assuming the transistor operate in saturation, neglecting body effect [1].

Transconductance:

$$Gm_{FDRFC} = gm_{1a}\left(1+K\right) \tag{1}$$

Output impedance:

$$Z_{out} \approx gm_8 r_{o8} r_{o10} // gm_6 r_{o6}\left(r_{o4a} // r_{o2a}\right) \tag{2}$$

Gain:

$$Av = -Gm_{FDRFC} Z_{out} \tag{3}$$

Thermal Noise:

$$\overline{V^2}_{T,in} = \frac{8kT\gamma}{gm_{1a}\left(1+K\right)} \cdot \left[\frac{\left(1+K^2\right)}{\left(1+K\right)} + \frac{gm_{3a}}{gm_{1a}} + \frac{gm_9}{gm_{1a}\left(1+K\right)}\right] \tag{4}$$

Where k is Boltzmann constant, T temperature and γ is a coefficient [10].

Flicker Noise:

$$\overline{V^2}_{f,in} = \frac{2K_P}{C_{ox}W_{1a}L_{1a}\left(1+K\right)f} \cdot \left[\frac{\left(1+K^2\right)}{\left(1+K\right)} + K\frac{K_N k_{PN}}{K_P k_{PP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{\left(K-1\right)}{\left(1+K\right)}\left(\frac{L_{1a}}{L_9}\right)^2\right] \tag{5}$$

Where K_P and K_N are process-dependent constants [10]. k_{PN} and k_{PP} are defined as the gate oxide capacitance per unit area C_{ox} multiplied by mobility of the respective carrier (μ_n or μ_p), electrons for NMOS and holes for PMOS.

C. Analysis of parameter K

In this subsection we show the analysis to obtain the optimal value for the parameter K in order to minimize the input-referred noise, maintaining a high gain and bandwidth.

1) Gain: The gain of the amplifier depends on its transconductance and output impedance. Equation (1) shows that the larger the parameter K the larger the transconductance. On the other hand, replacing $r_o = \frac{1}{\lambda I_D}$ and $gm = \frac{2I_D}{V_{ov}}$, where V_{ov} is the overdrive voltage, in Equation (2) shows that the smaller the parameter K the larger the output impedance. This is shown in the next equation.

$$Z_{out} = \frac{1}{V_{ov8}\lambda_8\lambda_{10}\left(K-1\right)\frac{I_b}{4}} // \frac{1}{V_{ov6}\left(\lambda_{2a}+K\lambda_{4a}\right)\lambda_6\frac{I_b}{2}} \tag{6}$$

After multiplying the transconductance and output impedance we obtain the following expression:

$$Av = -\frac{gm_{1a}\left(K+1\right)}{\frac{I_b}{2}} \cdot \left[\frac{1}{V_{ov8}\lambda_8\lambda_{10}\frac{\left(K-1\right)}{2} + V_{ov6}\left(\lambda_{2a}+K\lambda_{4a}\right)\lambda_6}\right] \tag{7}$$

The expression shows that the gain increases for K close to one, with K greater than one. However, a small value of K reduces the slew rate [1].

2) Thermal noise: For this analysis we refer to Equation (4) and to the relation of gm. Depending on the value of V_{ov} a transistor operate in weak, moderate or strong inversion. For transistors M3a, M3b, M4a, M4b, M9 and M10, we choose a large V_{ov} to ensure transistors operate in strong inversion and reduce the thermal noise. Nevertheless, transistors of the differential pair need to operate in weak inversion, with a small V_{ov} for increasing transconductance and gain. By design, V_{ov3a} is approximately equal to V_{ov9}, which is greater than V_{ov1a}. Considering this in equation (4) and taking the

derivative we obtain:

$$\frac{\partial \overline{V^2}_{T,in}}{\partial K} = -\frac{8kT\gamma}{gm_{1a}} \left[\frac{\left(\frac{K^2+2K-1}{K}\right)\frac{gm_{3a}}{gm_{1a}} - 2K + 2}{(K+1)^3} \right] \quad (8)$$

In order to calculate the minimum, (8) is equalled to zero and we find the value of K for the minimum thermal noise, discarding the negative root:

$$K = \frac{\sqrt{2\left(\frac{gm_{3a}}{gm_{1a}}\right)^2 + 1} - \frac{gm_{3a}}{gm_{1a}} - 1}{\frac{gm_{3a}}{gm_{1a}} - 2} \quad (9)$$

Equation (9) can be rewritten in an alternate form:

$$K = \frac{\frac{gm_{3a}}{gm_{1a}}}{\sqrt{2\left(\frac{gm_{3a}}{gm_{1a}}\right)^2 + 1} + \frac{gm_{3a}}{gm_{1a}} + 1} \quad (10)$$

As we can see in the expression, thermal noise is minimized for K smaller than one, however, this is not possible since K must be greater than one. We should choose a K as smaller as possible but greater than one.

3) Flicker noise: For this analysis we refer to Equation (5), which requires transistors M3a, M4a, M9 and M10 to have long channels to reduce flicker noise. Moreover, M1a, M1b, M2a and M2b require wide and short-channel transistors in order to have a large transconductance for the amplifier. By design, $L_9 \gg L_{1a}$, in addition, we can see $\frac{(K-1)}{(1+K)} < 1$. Hence, the term $\left[\left(\frac{K-1}{1+K}\right)\left(\frac{L_{1a}}{L_9}\right)^2\right]$ is neglected. Now, taking the derivative of Equation (5) we obtain:

$$\frac{\partial \overline{V^2}_{f,in}}{\partial K} = \frac{2K_P}{C_{ox}W_{1a}L_{1a}f} \quad (11)$$

$$\cdot \left[\frac{(K+1)\frac{K_N k_{PN}}{K_P k_{PP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2 + 2K - 2}{(K+1)^3} \right] \quad (12)$$

In order to calculate the minimum, (12) is equalled to zero and we find the value of K for the minimum flicker noise:

$$K = \frac{2 - \left[\frac{K_N k_{PN}}{K_P k_{PP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2\right]}{\left[\frac{K_N k_{PN}}{K_P k_{PP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2\right] + 2} \quad (13)$$

We can see in Equation (13), as it happens with thermal noise, the flicker noise is minimized for K smaller than one, but we choose a K greater and close to one.

III. Simulations Results

The amplifiers have been designed using the *AMS* 0.35 μm CMOS process, with V_{DD}=3.3V and simulated using Cadence. An open-loop analysis is realized to compare the gain, phase and input-referred noise between amplifiers with K=1.5, 2, 3 and 5.

Figure 2 and Figure 3 show the frequency response of the designed amplifiers. In Figure 2 we can see that the amplifier with highest open-loop gain is the FDRFC with smallest K at expense of a smaller bandwidth. For the required bandwidth (6 kHz) the gain is the highest for the largest K but all of the amplifiers still have an acceptable gain (more than 40 dB). The open-loop phase exhibits a zero for high frequencies that

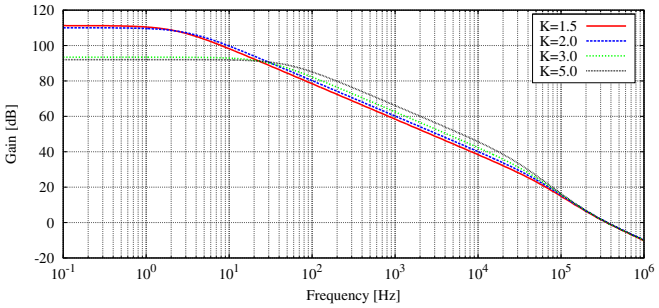

Fig. 2. Open-loop gain of FDRFC for different values of K.

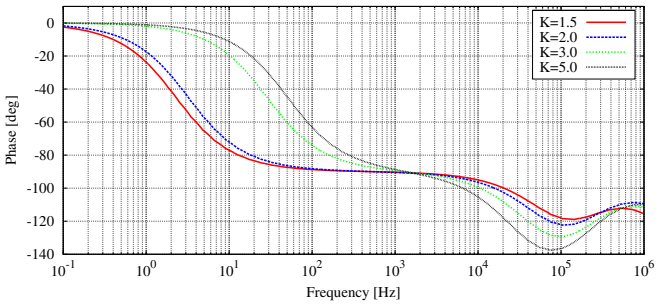

Fig. 3. Open-loop phase of FDRFC for different values of K.

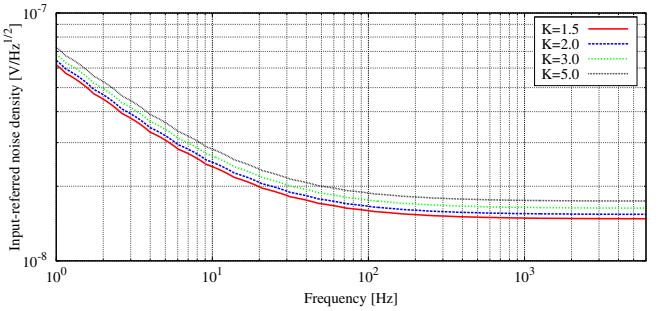

Fig. 4. Input-referred noise of FDRFC for different values of K.

TABLE I
SIMULATED OPERATING CONDITIONS AND SIZE FOR TRANSISTORS IN THE FDRFC AMPLIFIER WITH K=1.5

Transistor	$I_D(\mu A)$	$\frac{W}{L}$	$W(\mu m)$	$L(\mu m)$	$gm(\mu S)$
M0	15.99	10	100	10	122.4
M1a,M2a	4.00	62.5	250	4	83.83
M1b,M2b	3.99	62.5	250	4	83.4
M3a,M4a	6.02	0.375	45	120	23.3
M3b,M4b	3.99	0.25	30	120	15.26
M5,M6	2.01	0.8	8	10	20.1
M7,M8	2.01	28	28	1	41.41
M9,M10	2.01	0.325	39	120	7.66
M11,M12	3.99	1	10	10	31.91

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

Parameter	**This Work (Simulations)**	Lopez [6]	Majidzadeh [7]	Wattanapanitch [8]
Architecture	**FDRFC(K=1.5)**	FDFC	Telescopic-cascode	Folded-cascode OTA
Open-loop gain[dB]	**111.25**	105	72.8	-
Closed-loop gain[dB]	**42.1**	33.98 (single stage)	39.4	49 - 66
Bandwidth[Hz]	**6023**	6000	7200	11700
Phase Margin[deg]	**67.75**	84	-	-
Input-referred noise(1Hz-6kHz)[μVrms]	**1.16**	1.9	3.5	5.4 - 11.2
NEF	**2.58**	5.1	3.35	4.4 - 5.9
Power[μW]	**66.03**	66	7.92	5.4 - 20
Supply current[μA]	**20**	20	4.4	3.98
Supply voltage[V]	**3.3**	3.3	1.8	1.8
Technology	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS

might affect the dynamics of the amplifiers, however, they were designed with the zero far from the required bandwidth (≈100 kHz) to avoid stability problems (see Figure 3). As estimated in our analysis of the thermal and flicker noise, a small value of K reduces the input-referred noise (see Figure 4).

Finally, a closed-loop analysis is realized for the FDRFC amplifier with K=1.5 (see Figure 5 and Table I) with closed-loop gain set to 40 dB, since we consider this amplifier to have the best performance out of the four designed. It achieves an input-referred noise of 1.16 μV_{rms} (1 Hz-6 kHz) while consuming 66.03 μW, which corresponds to NEF=2.58 [9]. The open-loop gain is 111.25 dB, the closed-loop gain is 42.10 dB with a bandwidth of 6.02 kHz. Table **??** summarizes the performance and compares it with previous works. The open-loop gain of the FDRFC is the highest among the previous works with similar closed-loop gain. The power consumption of our amplifier is higher, nevertheless, the input-referred noise is 39% smaller than the state-of-the-art.

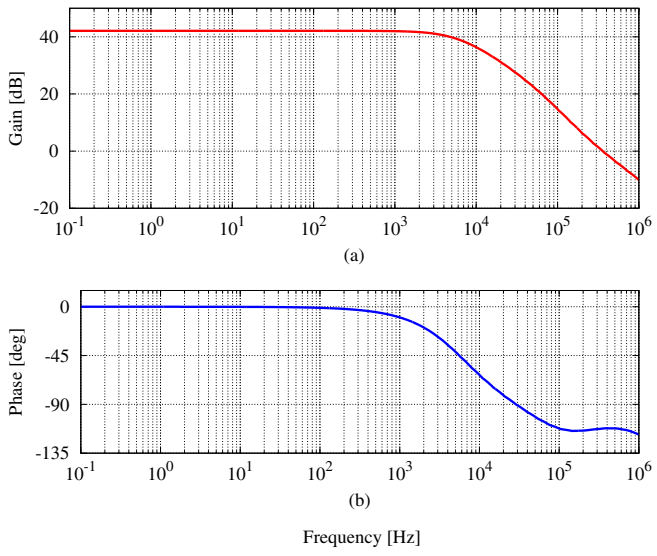

Fig. 5. Closed-loop frequency response for FDRFC with K=1.5. (a) Magnitude. (b) Phase.

IV. CONCLUSION

The recycling architecture was adapted successfully to obtain a low noise differential amplifier for a neural acquisition system. It achieves an input-referred noise of 1.16 μV_{rms} which is smaller than extracellular and electrode noise. It has been shown that a small value of K reduces the input-referred noise at the expenses of a smaller bandwidth. However this bandwidth is still higher than the required bandwidth for neural amplifiers. It is important to note that the recycling path (current mirrors M3a-M3b and M4a-M4b) add a pole-zero pair which might generate stability problems, therefore, it must be placed far from the frequencies of interest.

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